Optimizing Ferroelectric Nanowire for enhanced capacitance sub 60mV/decade subthreshold slope 

( in progress – completion: Summer 2020 )

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Introduction

Disclaimer: This research is in progress, until August 2020. The conclusions herein are from observations and analysis of verified simulation results thus far of the Ferroelectric material and device.

Introduction

As Moore’s (Denard’s) scaling law reach their limits due to short channel effects, methods for increasing computational density and IC performance without scaling device size are necessary.

Ferroelectric material exhibits two unique properties:
1. spontaneous polarization which enables an effective enhanced/negative capacitance. A large, or negative oxide capacitance improves a transistors subthreshold slope, making it a “more-ideal” switch.

2. Remnant polarization without the presence of an external Electric Field which enables Non-Volatile Memory Applications.

This research provides a detailed exploration of the fields and behavior of a ferroelectric capacitor, ferroelectric-oxide interface, and ferroelectric material integrated on the gate of a nanowire-FET to achieve sub 60mV/decade sub-threshold slope.

Methodology

Analysis Progression

To understand Ferroelectric material behavior, outline plots used to study Electrostatic Potential, Electric Field, FEPolarization, etc. across an isolated Ferroelectric capacitor.

Addition of SiO2 layer to study SiO2 and Ferroelectric interface

Placing FExSiO2 CAP onto junctionless nanowire to see how regions of enhanced and negative capacitance effect subthreshold slope and idv behavior in FeNW

Run Splits and optimize geometry for S.S.

2D planar structure created in device-editor. 2D planar simulation with AreaFactor=2 used to run many faster simulations and modify DOE iteratively. Cylindrical coordinates used with the planar structure for complete 3D device simulation about the Y=0 axis.

Troubleshooting and Verification

During simulation and analysis of the ferroelectric CAP, the electric field and Polarization in the Ferroelectric capacitor was non-constant and noisy when interfacing with SiO2. Upon debugging, a problem discovered in the TCAD software (2018 rel-P) did not correctly solve the Ferroelectric Polarization field when interfacing with Oxide. Synopsis new release re-Q, solves this problem with a: computableFEPolarization and FEPolarization=1.0 in Device Math Section.

Analysis and Results

To verify correct modeling of Ferroelectric layer and for careful study of ferroelectric, oxide and Silicon capacitance:

\[ C_g = \frac{q}{dV/dg} \]

from transient simulation is compared with Cfb= C_FE in series with C_SiO2, where

\[ C_FE = dFEPolarization \] / \( \delta V \)

Voltage enhancement across the Ferroelectric layer when integrated in a Nanowire (FeNW), enables voltage controlled negative FE layer Capacitance, and enhanced gate capacitance in series with oxide

Summary of Current Results

- Greater IF/EXO ratio, gives greater enhanced capacitance and will improve subthreshold slope.
- Greater FE increases Voltage drop across the Ferroelectric layer.

TO BE DONE:
- While curves of FeNW need to be verified to show negative capacitance gives sub 60mV/decade S.S.
- Negative Capacitance has been found for certain thickness splits over a Vg range. More splits will be run, to export, analyze and derive relationship for Vth and Subthreshold slope of the FeNW as a function of ferroelectric, oxide and substrate thickness.

Key References


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