December 6th, 2013		Fall 2013	MSEE Project/Thesis Final Presentation
Time	**Advisor**	**Presenter**	**Title**
		TRACK 1 - Room E345	
TR1/S1 9:00 - 9:25	Nader Mir	Akhil Vijendra & Swapnil Deshpande	Application of Software Defined Networking (SDN) for Router Functionality
TR1/S2 9:25 - 9:50	Nader Mir	Priyank Kothari and Abhinav Sharma	Power Consumption & Energy Efficiency in the Backbone networks Backbone networks
TR1/S3 9:50 - 10:15	Nader Mir	Ayeesri Muthumani & Renuka Radhakrishnan	Application of SDN for Multimedia Networks
TR1/S4 10:15 - 10:40	Lili He	Koushalya Ramakanth	ADC and DAC based Phase Locked Loop
Break - 10 min			
TR1/S5 10:50 - 11:30	Shahab Ardalan	Alfred Sargezisardrud [Thesis]	Delay Flip-Flop (DFF) Metastability impact on Clock , Data Recovery (CDR) and Phase-Locked Loop (PLL) circuits
TR1/S6 11:30 - 12:10	Shahab Ardalan	Muhammad Z. Ali [Thesis]	Low Power Analog To Digital Converter Design For Software Defined Radio's
TR1/S7 12:10 - 12:35	Shahab Ardalan	Natalia Lo	CMOS Clock Generator & Serializer
Break 10 min			
TR1/S8 12:45 - 13:10	Ping Hsu	Tony Beukers	High Speed and High Efficiency Space Vector Modulation Methods for a Three-Level Inverter
TR1/S9 13:10 - 13:35	Frank Lin	Brian Simpliciano	Biometric Fingerprint Cryptography Key Generation
TR1/S10 13:35 - 14: 00	Birsen Sirkeci	Ritchie Buenviaje	Use of Multiple Data Stream OFDM in Competitive Wireless Environments
TR1/S11 14:00 - 14:25	Robert Morelos	Lenny Rayzman	Crosstalk Mitigation to Reduce Bit Error Rate on Multi-Lane Multi-gigabit P C Board Interconnects
Break 10 min			
TR1/S12 14:35 - 15: 00	Robert Morelos	Keshava M. Elliadka	Unequal Error Protection with RaptorQ Codes
TR1/S13 15:00 - 15: 25	Peter Reischl	David Solomon	Implementation of Root Locus on Time Delayed Systems Using MATLAB
TR1/S14 15:25 - 15:50	Peter Reischl	Junaid Fatehi	Comparison of Predicted & Measured Energy From Photovoltaic Systems
TR1/S15 15:50 - 16:30	Peter Reischl	David Adams [Thesis]	"Real-time Auto Tuning of a Closed Loop Second Order System with Internal Time Delay Using Pseudo Random Binary Sequences"
		TRACK 2 - Room E340	
TR2/S1 9:00 - 9:25	Morris Jones	Vidhushini Sankar	A Distributed Light Weight Directory Access Protocol

TR2/S2 9:25 - 9:50	Morris Jones	Kunal Mali	A power efficient multilevel cache system for multicore
TR2/S3 9:50 - 10:15	Morris Jones	Renoy John Marattukalam & Santhosh Jayashankar	An In-depth Analysis of OpenFlow network using Mininet
TR1/S4 10:15- 10:40	Tri Caohuu	John Edwards	Toward an Efficient Library for Asynchronous Circuit Design
Break 10 min			
TR2/S5 10:50 - 11:15	Chang Choo	Babak Hashemizadeh & Kavoos Hedayati	FPGA Implementation of Basic Traffic Data Collection System
TR2/S6 11:15 - 11:40	Chang Choo	In-hwan Kim, Young-uk Chang	Accelerated Real Time Speech Recognition System using MFCC and DNN on FPGA
TR2/S7 11:40 - 12:05	Chang Choo	Hitesh Gannu and Tarun Tej Velaga	FPGA Based Simple Speech Recognition System
TR2/S8 12:05 - 12:30	Chang Choo	John Van Artsdalen & Rajshekar Kacharla	Simple Speech Recognition System on a Zynq SoC
Break 10 min			
TR2/S9 12:40 - 13:05	Chang Choo	Sparsh Patwa and Raafay Ahmad Khan	A Hardware Based Real Time Face Detection and Tracking System
TR2/S10 13:05 - 13:30	Chang Choo	Alex Huang	Object Detection in Ultrasound Elastography for Use in HIFU Treatment
TR2/S11 13:30 - 13: 55	Chang Choo	Adnan Tanwir & Suchindran K Ravi	Implementation of a robust face detection algorithm on a low cost FPGA
TR2/S12 13:55 - 14:20	Chang Choo	Ailing Ting and Shiyu Xu	Implementation of Nios II Based Multi Softcore System on Altera FPGA for Efficient Matrix Multiplication