SJSU Electrial Engineering Masters Presentations Dec 02, 2011

Track 1a **Room** 345 **Chair** He — Micro electronics

Time	Presenter1	Presenter2	Title
09:00:00 AM	Raymond Ng		Design of ring Voltage Control Oscillator for 800MHz in TSMC 0.25um
09:25:00 AM	Mingying Yang		Cadence Pcell Generation System
09:50:00 AM	Pratik Dahale		A High Speed Low Cost PLL for RF Applications
10:15:00 AM	Gaurav P. Chandawale		High Efficiency Solar Cell

Track 1b **Room** 345 **Chair** Hamedi hagh — Mixed Signal

Time	Presenter1	Presenter2	Title
11:00:00 AM	Hardik V Shah		HIHO Viterbi decoder
11:25:00 AM	Harmanpreet Singh Nanda		Design of a switched capacitor based sigma-delta modulator
11:50:00 AM	Abhiram Rudrapatna Sridhar		A Class D audio amplifier driver based on Sigma-Delta modulation (SDM)
12:15:00 PM	Scott Echols		Low-Power PLL in 45 nm CMOS

Track 1c **Room** 345 **Chair** Ardalan — VLSI and Mixed Signal

Time	Presenter1	Presenter2	Title
01:00:00 PM	Sameer Tamhankar		32 Bit Single Precision Floating Point Unit
01:25:00 PM	Bhairav Desai	Manan Patel	3 DES based Crypto-Processor
01:50:00 PM	Purviben Patel	Pallavi Shinde	Implementation of a robust ECC and AES cryptography algorithms
02:15:00 PM	Kedar Patel		Design of a Low Power, Low Voltage ADC for Biomedical Application

Track 1d **Room** 345 **Chair** Parent — Power and Neural

Time	Presenter1	Presenter2	Title
03:00:00 PM	Vikash Kumar		Design of a Magnetic Simulator Circuit for In-Vitro Neural Simulation System
03:25:00 PM	Ian Lopez Aguilar	Miranda	A First Step for a Real Time Auto-System Identification
03:50:00 PM	Albert Ng		Phase-Locked Loop for Quadratic Integrate and Fire Neuron
04:15:00 PM	Yin Wu		D/A Converter for Artificial Neuron

SJSU Electrial Engineering Masters Presentations Dec 02, 2011

Track 2a **Room** 343 **Chair** Le — Random numbers

Time	Presenter1	Presenter2	Title
09:00:00 AM	Satish S. Nair		Hardware implementation of exponential Variate generator (EVG)
09:25:00 AM	Parth Patel		Hardware Implementation of Binary Logarithm Function
09:50:00 AM	PANCHANAM SRI HARSHA		Hardware implementation of Gaussian variate generator

Track 2b **Room** 343 **Chair** Le — Random numbers, DSP, and energy

Time	Presenter1	Presenter2	Title
11:00:00 AM	Sergio de Ornelas		Crowd Energy Harvesting at Major Sporting Events
11:25:00 AM	Deepesh Bagmar		Hardware implementation of Linear Congruential Generator (LCG)
11:50:00 AM	Sricharan Narayanan		Hardware Implementation of Mersenne Twister
12:15:00 PM	Drupa Desai		2D-DCT Transform Implementation for H.264/AVC

Track 2c **Room** 343 **Chair** Choo — Video and FPGA I

Time	Presenter1	Presenter2	Title
01:00:00 PM	Ashwinkumar Gummaraju	Vaibhav Rushikesh Purani	Comparative Evaluation OF H.264 and VP8 Video CODEC
01:25:00 PM	Bhawandeep Singh Harsh		A hybrid hardware multithreading technique
01:50:00 PM	Nimit Pandya	Bhavika Patel	FPGA Implementation of an Edge Enhancing Smoothening Filter and Its
02:15:00 PM	Animesh Maurya		Rapid prototyping of a Real-time Human Motion Detection System on FPGA

Track 2d **Room** 343 **Chair** Choo — Video and FPGA II

Time	Presenter1	Presenter2	Title
03:00:00 PM	Sharanjit Singh	Navjot Singh	Design and Implementation of an FT-RLS Adaptive Filtering Algorithm on
03:25:00 PM	Pratik Talole		Generic Real Time Acquisition and Processing of Spectral Domain Medical
03:50:00 PM	Arun Kumar Thangavel	Firoz Dang	FPGA based Web Server
04:15:00 PM	Geethanjali Rajegowda		Efficient Implementation of RLS adaptive filter on FPGA

SJSU Electrial Engineering Masters Presentations Dec 02, 2011

Track 3a **Room** 343 **Chair** Jones — MISC I

Time	Presenter1	Presenter2	Title
09:00:00 AM	Mohmadshahid Kagathara	Sriram Natrajan	PCI Express Architecture for Embedded Applications
09:25:00 AM	Ankit Bhargava		Lagged-Fibonacci plus LFSR psudo random number generator
09:50:00 AM	Keyur Gajjar		Low Noise and Low Power Feed Forward Delta-Sigma Fractional-N PLL

Track 3b **Room** 341 **Chair** Mir — Networking I

Time	Presenter1	Presenter2	Title
11:00:00 AM	Sushant Wadhawan	Manoj Devpura	Implementation and Stimulation of Multicasting protocol using Network
11:25:00 AM	Heng Gao	Chaitra Shivakumar	Design and performance evaluation of IMS network using NS2
11:50:00 AM	Tejas Patel	Jinesh Patel	Design and Analysis of SIP

Track 3c **Room** 341 **Chair** Jones — VLSI and Networking

Time	Presenter1	Presenter2	Title
01:00:00 PM	Suviena Agarwal	Sagar Gawari	Hand-offs in a Mobile Environment
01:25:00 PM	Tosha Pandya		A Low Power 32-Bit ALU Design
01:50:00 PM	Premraj Patil		Bandwidth Optimization using Traffic shaping
02:15:00 PM	Venkatraman Swaminathan		Design and Layout of a 10-bit First Order Delta Sigma Modulator

Track 3d **Room** 341 **Chair** Jones — Networking II

Time	Presenter1	Presenter2	Title
03:00:00 PM	Ragavendra Prasad Murali	Prasanna Sridharan	Video Surveillance Using Live Stream On Android
03:25:00 PM	Pritish Somvanshi		IP Traceback to prevent DoS Attack
03:50:00 PM	Amit Radhakrishnan		Processor for High Speed IPv6 Header Parsing
04:15:00 PM	Phoebe Poon		Variable size 2D image scaler design using Finite Impulse Response (FIR)