Community Based Verification using UVM

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Methodology

Discussion

As a part of DUTs community, a collection 256-point complex FFT designs are taken to verify functionality using this approach. All FFT designs have same functionality with same design specification. Here, this 256-point complex design has 20 bits of real inputs and 20 bits of imaginary inputs. On the output, it has 20 bits of real outputs and 20 bits of imaginary outputs. As mentioned, UVM based test environment developed for verification of this complex DUT with a new approach.

FTT Sequence class

FTT sequence is not a UVM component, but it’s a UVM object. FTT sequence is responsible for all sequences that are generated for simulating the FTT DUT. All the test scenarios are covered through these sequences.

Sequences are generated in direct manner, randomized manner and constraint randomize manner. Some direct sequences are generated to cover some specific test scenarios. Constraint random sequences are generated to cover all remaining scenarios. Randomization of sequences is done through randomize() method. Randomization can be Pre-randomization or Post-randomization. Constraints are used to limit randomization as per test requirement and not to flood with not required randomized data.

FTT sequence uses start_item() method to send sequences to FTT driver through FTT sequence. This start_item() method is a blocking call and waits till it receives acknowledgement from driver.

FTT sequence finishes_item() method to end a transaction and to indicate to start a new transaction using start_item().

FTT Scoreboard module

In FTT scoreboard, each packet from input monitor consists of 3 fields: startin, realin, imagin. Data. Whole packet from result monitor consists of 3 fields: startout, realout, imagout. Input monitor and output monitor sends data as a single packet through uvm_analysis port. Input monitor sends pin level activity of input ports to scoreboard, while result monitor sends pin level activity of output ports to scoreboard. Scoreboard receives these packets through tfm_analysis_fifo. Two fifo defenses; one for input monitor packets and another for result monitor packets. All reporting is done in scoreboard. For reporting purpose, uvm_info, uvm_fatal, uvm_error and uvm_warning. These reporting macros done in all UVM components. All these macro results are captured and used for reporting purpose.

FFT scoreboard is a UVM component that is responsible for all checking. As earlier mentioned, UVM is a message-based verification methodology. So UVM components communicates with each other using messages. Here, scoreboard receives data packets from different monitors and performs checking on that data.

Analysis and Results

FFT DUT community functionally verified and results are analyzed for segregation of good DUTs and bad DUTs. Here, for each DUT results are captured and kept it for a comparison with other DUT result. 18 FFT DUTs has been verified using this approach.

Out of 18 FFT DUTs, one good DUT and one bad DUT result is shown in these figures. Above result and waveform shows a good DUT that been identified after result analysis of all DUTs.

Result analysis is done with results comparison. Identification of good DUT is done based on which area it belongs. If result of a DUT belongs to major area of result, which is more than 50% DUTs has same results. DUTs which belongs to lesser area of results are identified as bad DUTs. There is no reference model to compare actual DUT results to expected results. That’s why community of results will work as a reference point for identification of DUTs within the community.

Summary/Conclusions

Community of FFT DUTs was successfully verified using this new approach of verification. This project concludes that verification with any reference model can be used for identifying bad designs from collection of same functionality designs. All the designs were verified with same set of test cases and results are logged for analysis.

As future scope of this project, community-based verification approach can be tested for performance verification of DUTs. Currently, this UVM based verification environment was developed for only functional verification.

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