Course Description

This course is a prerequisite for all electronics area courses and reviews semiconductor device physics and technology. The students are expected to have some background in atomic physics and solid state physics for this course. The course is divided into four parts—semiconductor fundamentals, p-n junctions, bipolar junction transistors (BJT), and field effect transistors (FET).

Course Goals and Student Learning Objectives

Upon successful completion of this course, students will be able to:

LO1 Describe fundamental concepts of solid-state physics applied to the semiconductor devices by Silicon and compound semiconductor materials.

LO2 Explain general electrical behavior of semiconductor Si and GaAs, construct appropriate physical models.

LO3 Illustrate structural details and current-voltage characteristics of p-n junction diode, BJT, MOSFET, Metal/semiconductor diode, and MESFET.

LO4 Apply the fundamental understandings of semiconductor devices with knowledge on the limitations of physical models.
Required Texts/Readings

Textbook


Other Readings


Classroom Protocol

Students are expected to participate actively in class. Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class.

Assignments and Grading Policy

a. Homework

Homework is assigned and will be posted online during the semester (usually one per chapter). Homework will be collected. The solution will be discussed in class and posted in the web.

b. Exams

There are two mid-term examinations and one final examination.

c. Class Participation:

Class participation is required, and student attendance will be checked.

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drops, academic renewal, etc. Information on add/drops are available at [http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html](http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html). Information about late drop is available at
http://www.sjsu.edu/sac/advising/latedrops/policy/. Students should be aware of the current deadlines and penalties for adding and dropping classes.

### Grading Policy

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Midterms (two)</td>
<td>25% each</td>
</tr>
<tr>
<td>Quiz and Class Participation</td>
<td>10%</td>
</tr>
<tr>
<td>Homework (online submission)</td>
<td>5%</td>
</tr>
<tr>
<td>Final Exam</td>
<td>35%</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>100%</strong></td>
</tr>
</tbody>
</table>

**Final Grade Percentage Breakdown**

- 90% and above: A
- 89% - 85%: A-
- 84% - 80%: B+
- 79% - 70%: B
- 69% - 65%: B-
- 64% - 60%: C+
- 59% - 55%: C
- 54% - 50%: C-
- 49% - 45%: D+
- 44% - 40%: D
- below 40%: F

### University Policies

**Academic integrity**

Students should know that the University’s [Academic Integrity Policy is available at](http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf). Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University’s integrity policy, require you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for Student Conduct and Ethical Development is available at [http://www.sa.sjsu.edu/judicial_affairs/index.html](http://www.sa.sjsu.edu/judicial_affairs/index.html).

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person’s ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this
class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that SJSU’s Academic Policy F06-1 requires approval of instructors.

**Campus Policy in Compliance with the American Disabilities Act**

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.
# EE221 / Principle of Semiconductor Devices, Section-1

## Spring 2017, Course Schedule

**Table 1 Tentative Course Schedule**

*The schedule is subject to change with fair notice to be announced in class.*

<table>
<thead>
<tr>
<th>Date</th>
<th>Topic</th>
<th>Reading</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/26</td>
<td>Class logistics and introduction to Semiconductor Devices and Technology</td>
<td>Chapter 0</td>
</tr>
<tr>
<td>1/31 &amp; 2/2</td>
<td>Semiconductor Energy Bands, and materials</td>
<td>Chapter 1: 1.1-2.2, 1.4-1.7</td>
</tr>
<tr>
<td>2/7 &amp; 2/9</td>
<td>Semiconductor Carrier Concentration</td>
<td>Chapter 1: 2.1-2.3</td>
</tr>
<tr>
<td>2/14 &amp; 2/16</td>
<td>Carrier transport</td>
<td>Chapter 2: 2.4-2.7</td>
</tr>
<tr>
<td>2/21 &amp; 2/23</td>
<td>p-n Junctions fabrication; equilibrium conditions</td>
<td>Chapter 3: 3.1-3.2</td>
</tr>
<tr>
<td>2/28 &amp; 3/2</td>
<td>p-n junction operation</td>
<td>Chapter 3: 3.3-3.4</td>
</tr>
<tr>
<td>3/7 &amp; 3/9</td>
<td>Review for 1st exam, 1st Mid-Exam, 3/9/17</td>
<td></td>
</tr>
<tr>
<td>3/14 &amp; 3/16</td>
<td>Discussion 1st exam results; Reverse breakdown, Hetero junctions</td>
<td>Chapter 3: 3.5-3.7</td>
</tr>
<tr>
<td>3/21 &amp; 3/23</td>
<td>Bipolar Transistor Fundamentals: The transistor action</td>
<td>Chapter 4: 4.1-4.2</td>
</tr>
<tr>
<td>3/27 &amp; 3/31</td>
<td>Spring Recess</td>
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</tr>
<tr>
<td>4/4 &amp; 4/6</td>
<td>Static Characteristics of BJT, Heterojunction BJT</td>
<td>Chapter 4: 4.3-4.4</td>
</tr>
<tr>
<td>4/11 &amp; 4/13</td>
<td>The MOS Diode, ideal MOS</td>
<td>Chapter 5: 5.1</td>
</tr>
<tr>
<td>4/18 &amp; 4/20</td>
<td>MOSFET fundamentals</td>
<td>Chapter 5: 5.2-5.5</td>
</tr>
<tr>
<td>5/2 &amp; 5/4</td>
<td>Discuss 2nd exam results; MOS Characteristics; MOS scaling, etc.</td>
<td>Chapter 6: 6.1-6.5</td>
</tr>
<tr>
<td>5/9 &amp; 5/11</td>
<td>Metal-Semiconductor contacts, MESFET</td>
<td>Chapter 7: 7.1-7.3</td>
</tr>
<tr>
<td>5/16</td>
<td>Review for final</td>
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</table>

**Final Examination:** 5/18/2017, Thursday, 2:45-5:00pm
The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

“I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- Take an exam in place of someone else, or have someone take an exam in my place
- Give information or receive information from another person during an exam
- Use more reference material during an exam than is allowed by the instructor
- Obtain a copy of an exam prior to the time it is given
- Alter an exam after it has been graded and then return it to the instructor for re-grading
- Leave the exam room without returning the exam to the instructor.”

Measures Dealing with Occurrences of Cheating

- Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.
- A student’s second offense in any course will result in a Department recommendation of suspension from the University.