San José State University  
Department of Electrical Engineering  
EE122, Electronic Design I  
Number 20214, Section 01, Spring 2017

Coordinator: Prof. Hamedi-Hagh  
Instructor: Prof. Hamedi-Hagh  
Office Location: ENGR381  
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Email: sotoudeh.hamedi-hagh@sjsu.edu  
Office Hours: Tuesdays 10:15 to 11:30 and 15:30 to 16:30  
Class Schedule: Tuesdays/Thursdays 9:00-10:15  
Classroom: ENGR345  
Prerequisites: EE110 and related background in circuit analysis, transient and frequency responses

Course Description
This course teaches the operation, modeling and analysis of basic electronic blocks and components such as operational amplifiers (opamps), diodes, metal oxide semiconductor (MOS) transistors. The design and characteristics of analog amplifiers and digital inverters are also studied. The laboratory experiments associated with this course involves circuit simulations using Spice and measurement.

Required Textbook:
The first eight chapters of the following textbook are covered in this course.  
  www.wiley.com/college/razavi  
  Chapter 1: Introduction to Microelectronics  
  Chapter 8: Operational Amplifiers as a Black Box  
  Chapter 2: Basic Physics of Semiconductors  
  Chapter 3: Diode Models and Circuits  
  Chapter 6: Physics of MOS Transistors  
  Chapter 7: CMOS Amplifiers

Other Reading for Reference Only:  
  www.sedrasmith.org/

Grades
Six Quizzes 6×2.5%  
Two Midterms 2×15%  
Final exam 30%  
Laboratory 25%  
Assignments 5% (extra bonus)

Grading Percentage Breakdown
90% and above A  
89% - 85% A-  
84% - 82% B+  
81% - 79% B  
78% - 75% B-  
74% - 72% C+
Exams and Grading Policy
There will be two midterm exams and a final exam. Exams are closed book. Students are allowed to bring a calculator and a page of formula. Final exam will be comprehensive. There will be no make-up exams (unless under a very special circumstance and when both written excuse and official proofs are provided). Exam solutions will be discussed in the class after the midterm exams.

Course Goals and Student Learning Objectives
Fundamental building blocks for Analog integrated circuits, basic physical electronics, electronic devices, and device characteristics. The devices include diodes, field-effect transistors (FET), and operational amplifiers (Opamps). Analysis (DC and small-signal) and circuit design containing diodes, FETs, and opamps.

GE/SJSU Studies Learning Outcomes (LO), if applicable
Upon successful completion of this course, students will be able to:
LO1: Demonstrate an understanding of the fundamentals of Electrical Engineering, including its mathematical and scientific principles, analysis and design.
LO2: Demonstrate the ability to apply the practice of Engineering in real-world problems.

Course Content Learning Outcomes
Upon successful completion of this course, students will be able to:
LO3: Apply the knowledge of mathematics, science, and engineering in circuit analysis (3.a)
LO4: Analyze and design integrated amplifier circuits to meet desired needs (3.c)
LO5: Identify, formulate, and solve engineering problems in Analog circuit design (3.e)
LO6: Demonstrate to use the techniques, skills, and modern engineering tools necessary for engineering practice (3.k)

ABET outcomes
The letters in parentheses in the course learning objectives refer to ABET criterion 3 outcomes satisfied by the course. These are listed below as a reference:
(a) An ability to apply knowledge of mathematics, science, and engineering
(b) An ability to design and conduct experiments, as well as to analyze and interpret data
(c) An ability to design a system, component, or process to meet desired needs
(d) An ability to function on multi-disciplinary teams
(e) An ability to identify, formulate, and solve engineering problems
(f) An understanding of professional and ethical responsibility
(g) An ability to communicate effectively
(h) The broad education necessary to understand the impact of engineering solutions in a global and societal context
(i) A recognition of the need for, and an ability to engage in life-long learning
(j) A knowledge of contemporary issues
(k) An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice
(l) Specialization in one or more technical specialties that meet the needs of companies
(m) Knowledge of probability and statistics, including applications to electrical engineering
(n) Knowledge of advanced mathematics, including differential and integral equations, linear algebra, complex variables, and discrete mathematics
(o) Basic sciences, computer science, and engineering sciences necessary to analyze and design complex electrical and electronic devices, software, and systems containing hardware and software components
Dropping and Adding
Students are responsible for understanding the policies and procedures about add/drops, academic renewal, etc. Students should be aware of the current deadlines and penalties for adding and dropping classes. Information on add/drops are available at http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html. Information on late drop is at http://www.sjsu.edu/sac/advising/latedrops/policy.

Projects and Homework:
Problem solution is essential for student’s success in this course and the textbook problems are all designed to better prepare students for examinations. Textbook provides answers to some chapter questions. It is highly recommended that students solve as many questions as possible and verify their answers during office hours. A number of projects will be assigned to the students in the laboratory part of this course, where a student will design, simulate, build, and test an electronic circuit, write a final report on the project and give a presentation. For more detail refer to EE124 Laboratory Manual.

University Policy in Academic integrity
Students should know that the University’s Academic Integrity Policy is available at http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf. Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University’s integrity policy, require you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for Student Conduct and Ethical Development is available at http://www.sa.sjsu.edu/judicial_affairs/index.html. Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person’s ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that SJSU’s Academic Policy F06-1 requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act
If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.
## Tentative Course Syllabus and Schedule

<table>
<thead>
<tr>
<th>Date</th>
<th>Topics</th>
</tr>
</thead>
<tbody>
<tr>
<td>01/26</td>
<td>Introduction and Review of Circuit Theory</td>
</tr>
<tr>
<td>01/31</td>
<td>Diode Operation, Biasing and Modeling</td>
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<tr>
<td>02/02</td>
<td>Diode Operation, Biasing and Modeling</td>
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<tr>
<td>02/07</td>
<td>Half-Wave and Full-Wave Rectifiers</td>
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<tr>
<td>02/09</td>
<td>Zener Diodes, Regulators and Logarithmic Amplifiers</td>
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<tr>
<td>02/14</td>
<td>Zener Diodes, Regulators and Logarithmic Amplifiers</td>
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<tr>
<td>02/16</td>
<td>Gain of Non-ideal Inverting and Noninverting Opamps</td>
</tr>
<tr>
<td>02/21</td>
<td>Input and Output Resistance of Non-ideal Opamps</td>
</tr>
<tr>
<td>02/23</td>
<td>EXAM I</td>
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<tr>
<td>02/28</td>
<td>Bandwidth of Non-ideal Inverting and Noninverting Opamps</td>
</tr>
<tr>
<td>03/02</td>
<td>Opamp Offset Voltage, Slew-Rate and Settling Time</td>
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<tr>
<td>03/07</td>
<td>Comparators and Inverting and Noninverting Hysteresis Circuits</td>
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<tr>
<td>03/09</td>
<td>Comparators and Inverting and Noninverting Hysteresis Circuits</td>
</tr>
<tr>
<td>03/14</td>
<td>Oscillators and Function Generators</td>
</tr>
<tr>
<td>03/16</td>
<td>MOSFET Operation</td>
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<tr>
<td>03/21</td>
<td>MOSFET Biasing and Modeling</td>
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<tr>
<td>03/23</td>
<td>MOSFET Biasing and Modeling</td>
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<tr>
<td>04/04</td>
<td>NMOS Common Source Amplifiers DC Analysis</td>
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<tr>
<td>04/06</td>
<td>PMOS Common Source Amplifiers DC Analysis</td>
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<tr>
<td>04/11</td>
<td>NMOS/PMOS Common Source Amplifiers AC Analysis</td>
</tr>
<tr>
<td>04/13</td>
<td>EXAM II</td>
</tr>
<tr>
<td>04/18</td>
<td>NMOS Common Gate Amplifiers DC Analysis</td>
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<tr>
<td>04/20</td>
<td>PMOS Common Gate Amplifiers DC Analysis</td>
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<td>04/25</td>
<td>NMOS/PMOS Common Gate Amplifiers AC Analysis</td>
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<tr>
<td>04/27</td>
<td>NMOS/PMOS Common Gate Amplifiers AC Analysis</td>
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<tr>
<td>05/02</td>
<td>NMOS/PMOS Common Drain Amplifiers DC Analysis</td>
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<tr>
<td>05/04</td>
<td>NMOS/PMOS Common Drain Amplifiers AC Analysis</td>
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<tr>
<td>05/09</td>
<td>NMOS/PMOS Source Degeneration Amplifiers</td>
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<tr>
<td>05/11</td>
<td>NMOS/PMOS Source Degeneration Amplifiers</td>
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<tr>
<td>05/16</td>
<td>MOS Switches and Digital Gates (optional)</td>
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<tr>
<td>05/17</td>
<td>Study/Conference Day (no class or exam)</td>
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<td>05/17</td>
<td>Assignment Submission Deadline, 5% Bonus Grade</td>
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<tr>
<td>05/23</td>
<td>FINAL EXAM (7:15 — 9:30), 30% Grade</td>
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Holidays: 03/27 to 03/31 (Spring Break)