San José State University  
College of Engineering

EE275 Advanced Computer Architecture  
Spring 2017, Section 1

Instructor: Prof. Chang “Charles” Choo, www.sjsu.edu/people/chang.choo
Office Location: Engineering Building Room 253
Telephone: (408) 924-3980
Email: chang.choo@sjsu.edu
Office Hours: Mon, Wed, noon-1pm
Class Days/Time: Mon, Wed 4:30pm-5:45pm
Classroom: ENG 189

Prerequisites: Basic computer organization and logic circuits; Hardware Description Language (Verilog or VHDL) for VLSI/ASIC/FPGA Program students in particular; High-level programming language (C/C++) for Networking Program students in particular; Assembly language programming preferred.

Course Format:
Course topics include performance metrics, instruction set architectures, instruction pipelining and pipeline hazards, instruction-level parallelism, multithreading, cache and virtual memory, I/O performance and advanced topics in storage systems, topologies and hardware/software issues of interconnection networks. There will be 4 mini-projects.

Required Texts

References
TBD

Web site (Canvas)
Class information, notices, course materials, FAQs (selected course related emails between students and Instructor) will be posted on the web. In addition, all the changes on the tentative list of homework problems (see below), as well as solutions to homework, will be available on the web. Students are urged to visit the web site twice a week.

**Exams and Assignments**
There will be one midterm and one final exam. There will be 4 mini-projects and 5-7 assignments.

**Office Hours**
The office hours are made available for questions about lectures and projects and for discussion of grades assigned. If you need a help of the instructor, see him right after class or during his office hours. Use of email is strongly recommended for other times, although appointments may be made for mutually convenient times.

**Grading Policy**
The weighting among exams, assignments, and homework will be:

- Mini-projects (4) 40%
- Homework 10%
- Midterm Exam 20%
- Final Exam 30%

**Tentative Course Schedule**

**Mini-Projects**

<table>
<thead>
<tr>
<th></th>
<th>Topic</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Pipelined floating-point adder design (Due: TBD)</td>
</tr>
<tr>
<td>2</td>
<td>Pipelined MIPS-like CPU design (Due: TBD)</td>
</tr>
<tr>
<td>3</td>
<td>Adding advanced features to previous design (Due: TBD)</td>
</tr>
<tr>
<td>4</td>
<td>Literature Survey on selected computer architectures (Due: TBD)</td>
</tr>
</tbody>
</table>

**Tentative Schedule**

<table>
<thead>
<tr>
<th>Lecture</th>
<th>Date</th>
<th>Topic</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1/30</td>
<td>Introduction</td>
</tr>
<tr>
<td>2</td>
<td>2/1</td>
<td>Arithmetic Circuit Review</td>
</tr>
</tbody>
</table>
IEEE Floating-point arithmetic circuits

History of Computing

Instruction set architecture

Addressing modes and instruction format, control sequencing,

Instruction pipeline

Performance measures

Memory hierarchy, memory organization

Cache memory design parameters

Cache memory system design

Virtual memory

Pipeline hazards, ILP

Forward chaining, branch prediction

Loop unrolling and software pipeline

Midterm, in-class

DLP, Vector processor

Memory interleaving

Multiprocessor and TLP

Cache coherence, MESI protocol

GPU architecture

GPU and CUDA

Heterogeneous computing

Warehouse-Scale Computers, Data Center,

Request-Level Parallelism (RLP)

Embedded system

AI architecture and DNN

DNN (cont’d)

Final Exam, 2:45pm-5pm

PLEASE DO NOT CONSUME FOOD IN THE CLASSROOM

EE@SJSU

Honesty and Respect for Others and Public Property

EE HONOR CODE

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

“I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

• Take an exam in place of someone else, or have someone take an exam in my place
• Give information or receive information from another person during an exam
• Use more reference material during an exam than is allowed by the instructor
• Obtain a copy of an exam prior to the time it is given
• Alter an exam after it has been graded and then return it to the instructor for re-grading
• Leave the exam room without returning the exam to the instructor.”

Measures Dealing with Occurrences of Cheating
• Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.
• A student’s second offense in any course will result in a Department recommendation of suspension from the University.

EE HONOR CODE
In addition to EE Honor Code, EE118 students understand that professional attitude is necessary to maintain a comfortable academic environment. For examples:
• I do not just skip the lecture and then ask the instructor to summarize the lecture for me later on. Office hours are for students to have questions, not for the instructor to summarize the lecture for any specific student.
• I come to the class on time and leave the class at the end of the lecture.
• To minimize possible tension during the exams, I WILL follow the exam rules closely.
• I work on the lab assignments and final project by myself.
• I understand that long-term learning is my responsibility and so I always keep it up.
• I strongly believe that NOT any statement similarly to examples below can be used:
  • I am working full-time and so do not have enough time for the class.
  • I have quite many classes this semester and so I do not have enough time for the class.
  • I just need a passing grade to graduate this semester.
  • I live far away from the campus and so I can not come to the class often.
• etc., etc....

(C.Choo, Last Updated 1/30/17)