(1/30) For Lab use, please download the Xilinx ISE Design Suite 14.7 Webpack from the website below. Note that you must register first before downloading.

http://xilinx.com/support/download/index.htm

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<th>Week of</th>
<th>Lab Activity (Pre-Lab work is required!)</th>
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<td>Experiment C – Familiarization of TTL ICs (Parts I &amp; II)</td>
<td>Familiarization of TTL ICs</td>
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<td>3</td>
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<td>Experiment A – Xilinx ISE Tools; Schematic Entry &amp; Simulation</td>
<td>Simple to moderately complex design schematic entry &amp; simulation</td>
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<td>4</td>
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<td>6</td>
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<td>Experiment E – Schematic Entry, Simulation and FPGA Demonstration of the 2-bit Comparators</td>
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<td>9 Apr 3</td>
<td>Experiment G – Flip-flops: Simulation (Part 1)</td>
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<td>10 Apr 10</td>
<td>Experiment G – Flip-flops: Hardwiring; Debouncing Circuit Design (Part 2)</td>
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<td>11 Apr 17</td>
<td>Experiment H – BCD Counter Design and Hardwiring</td>
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<td>12 Apr 24</td>
<td>Experiment I – Design &amp; Demo of HEX Counter Using Artix FPGA Board</td>
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<td>13 May 1</td>
<td>Experiment J – Traffic Light Controller (FF-based, “Richards Controller”-based, or verilog/FPGA)</td>
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<td>14 May 8</td>
<td>Final Exam (in-class)</td>
<td>Part I: Written Part II: Demo</td>
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**DIGITAL LOGIC CIRCUIT DESIGN — LAB**
COURSE: EE118 Lab - Digital Logic Circuit Design Laboratory (ENG305) Coordinated by Prof. Choo, and taught by

EE118-02: Thu, 9am-11:45am, ENG-305(Lab), taught by
Raaj Vora

EE118-03: Thu, 6pm-8:45pm, ENG-305(Lab), taught by
Raj Pednekar

EE118-04: Tue, 1:30pm-4:15pm, ENG-305(Lab), taught by
Dhruv Thakkar

EE118-05: Tue, 1:30pm-4:15pm, ENG-305(Lab), taught by
TBA

Course Outcomes:
The goals of this laboratory course is:

1. To apply concepts and methods of digital circuit design techniques as discussed in the class (EE118) through hands-on lab modules. [a]
2. Learn to design combinational and sequential digital systems starting from a word description that performs a set of specified tasks and functions. [c]
3. To analyze the results of logic and timing simulations and to use these simulation results to debug digital systems. [b]
4. Develop skills, techniques and learn state-of-the-art engineering tools (such as Verilog, Xilinx tools) to design, implement and test modern-day digital systems on FPGAs. Traditional “hard-wiring” on a breadboard using discrete (TTL) components will also be practiced in appropriate labs [i]
5. Learning through hands-on experimentation the Xilinx tools for FPGA design as well as the basics of Verilog to design and simulate digital systems. [k]

CO-REQUISITE: EE118


REFERENCES: Xilinx, ISE Student Edition 14.7, (Xilinx schematic capture and simulation software; Lab PCs have this software installed. Also may be downloaded from Xilinx website).
WEB SITE: Class information, notices, course materials, FAQs (selected course-related e-mails between students and instructors) will be posted on the Canvas. In addition, all the changes on the tentative list of homework problems (see below), as well as solutions to homework, will be available on the web. Students are urged to visit the web site at least twice a week.

EVALUATION: The weighting among lab performance, midterm, and final project

- Lab report, demo & pre-lab report, quiz, if any
  - 10 labs: 6% for each lab
- Final Exam (or Project): 25%
- Midterm: 15%

EXAMS: There will be a midterm and a final exam or project in the lab.

OFFICE HOURS: Your lab instructor has office hour to be posted.

HELP SESSION: Weekly help sessions will be provided by your lab instructor. The sessions will be: TBA in IEEE Room.

Lab Report Writing Guidelines: Each student has to submit a report for each session. The main objective for the report is to communicate the results to others and to enable others to duplicate the work in a straight-forward manner.

When preparing the lab report, you should use a word processor (it will save you time to have a template that you follow for each lab, according to the guidelines described below). You have to include printouts of all logic schematics, simulated waveforms, and Verilog code listings, if any. The lab report does not need to be step-by-step detailed, but should show that you have a good understanding of the lab. Also, the lab report should be complete, where all information requested should be in the lab report. For each lab, the listing of the report requirements will be presented during the lab lecture, and will be posted on the lab website, if necessary.

Reports are to be either neatly hand-written or, preferably, typed (or a combination of both) and should contain the following information. A report should be concise but thorough. The length of a typical report should not exceed 10 pages. The lab report is due at the start of the next lab.

1. Title, date and name of the student.
2. Follow the following format (The report counts for 70 points
out of a total of 100 points per lab. Remaining 30 points is for successful demonstration, if any)

1. Pre-lab: (15 points, unless otherwise indicated - these are usually given for the on-line answers and done by each student)

For the questions which are not submitted on-line, include schematics (if appropriate), a brief explanation of the circuit and derivations (or optimizations/simplifications, K-maps if applicable) to the questions. However, questions which were submitted on-line need not be included in the report.

2. Introduction (10 pts)

Give the goals/objectives of the lab experiment.

3. Theory of Operation and explanation of the design

Give a brief discussion of the theory of operation, including schematics and equation used, etc. This is of particular importance for the design-oriented labs. You should also explain the schematics involved in your design.

4. Experimental results: (70 points including the section on "Theory of Operation" unless otherwise indicated)

   a. Brief description of the lab experiment.

   b. Schematics of the circuit (from Xilinx schematic entry tool). Put your name and date on each page.

   c. Simulated waveform.

   d. Discussion of the results indicating that the circuit functions properly. It is not good enough to just give the simulated waveform. It is up to you to show that this waveform correspond to what you expect (do not say "The simulation shows that the circuit works properly"). You need to make it clear to the reader that the circuits work properly! One convenient way is to give a truth table and indicate that for each entry the corresponding
values given by the logic simulator by labeling the simulated waveforms. Include also a reasonable detailed discussion of the results.

5. Conclusion. (15 points, unless otherwise indicated)

This is an important part of the report. The conclusion should contain a summary of the results. Are the goals of the lab fulfilled? If not, explain why.

6. Sign and date the entry

3. Neatness, organization and presentation: 5 points

CLASS ATTENDANCE:

Attendance at lecture is strongly recommended.

PLEASE DO NOT CONSUME FOOD IN THE CLASSROOM

EE@SJSU

Honesty and Respect for Others and Public Property

EE HONOR CODE

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

“I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

• Take an exam in place of someone else, or have someone take an exam in my place
• Give information or receive information from another person during an exam
• Use more reference material during an exam than is allowed by the instructor
• Obtain a copy of an exam prior to the time it is given
• Alter an exam after it has been graded and then return it to the instructor for re-grading
• Leave the exam room without returning the exam to the instructor.”

Measures Dealing with Occurrences of Cheating

• Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.
• A student’s second offense in any course will result in a Department recommendation of suspension from the University.

EE HONOR CODE

In addition to EE Honor Code, EE118 students understand that professional attitude is necessary to maintain a comfortable academic environment. For examples:

• I do not just skip the lecture and then ask the instructor to summarize the lecture for me later on.
Office hours are for students to have questions, not for the instructor to summarize the lecture for any specific student.

- I come to the class on time and leave the class at the end of the lecture.
- To minimize possible tension during the exams, I WILL follow the exam rules closely.
- I work on the lab assignments and final project by myself.
- I understand that long-term learning is my responsibility and so I always keep it up.
- I strongly believe that NOT any statement similarly to examples below can be used:
  - I am working full-time and so do not have enough time for the class.
  - I have quite many classes this semester and so I do not have enough time for the class.
  - I just need a passing grade to graduate this semester.
  - I live far away from the campus and so I can not come to the class often.
  - etc., etc....