1. Course Information
Instructor: Tamara Schmitz (Dr. T)
Department: Electrical Engineering
College of Engineering, San Jose State University.
Spring Semester, 2007

<table>
<thead>
<tr>
<th>Course Title:</th>
<th>Test Development Engineering I</th>
</tr>
</thead>
<tbody>
<tr>
<td>Course Code:</td>
<td>EE182</td>
</tr>
<tr>
<td>Section:</td>
<td>01</td>
</tr>
<tr>
<td>Class Hours &amp; Location:</td>
<td>2:30 – 4:30pm in MIST lab</td>
</tr>
<tr>
<td>Office Hours:</td>
<td>M 11-1, T 10-11:30, W 11-12</td>
</tr>
<tr>
<td>Office Location:</td>
<td>E365</td>
</tr>
<tr>
<td>Office Phone:</td>
<td>924-3989</td>
</tr>
<tr>
<td>E-mail:</td>
<td><a href="mailto:schmitzor@gmail.com">schmitzor@gmail.com</a></td>
</tr>
<tr>
<td>Preferred Contact: (Either through email or Phone)</td>
<td>Email, just email</td>
</tr>
<tr>
<td>Department Fax:</td>
<td>(408) 924-3925</td>
</tr>
</tbody>
</table>

2. Course Description:
a. Course Overview and Description:
Present the basics of test development engineering in a benchtop test environment. The per-pin architecture of a manufacturing tester is modeled by a printed circuit board designed especially for the class. Each section of that architecture is tested separately and in total, including voltage regulators, operational amplifiers, digital-to-analog converters, and analog-to-digital converters.

b. Prerequisites:
EE122 and consent of the instructor

c. Required and recommended texts, readers, or other reading materials:
- App Notes and Data Sheets from Industry

d. Other Reading materials: none

e. Student learning objectives for the course:
The students should be able to
1. Solder through-hole and surface mounts components on pre-made printed circuit board
2. Perform basic DC measurements on components and integrated circuits
3. Apply techniques of calibration and correction to achieve a given measurement accuracy
4. Understand the advantages of DSP-based testing
5. Explain the issues involved in test economics and motivation for Design for Test (DFT)
6. Test, measure, and analyze data from voltage regulators, op amps, DACs and ADCs.
7. Design, solder, and measure an evaluation board for an current industry IC

3. Course requirements:
a. Projects: multiple labs, final project
b. Exams: one midterm exam
c. Quizzes: yes
d. Homework: lab work
e. Class Participation: yes, lab notebook, station log notebook
### 4. Tentative course calendar: (Please note that the course calendar is “subject to change with fair notice”)

<table>
<thead>
<tr>
<th>Week</th>
<th>Topics</th>
<th>Reading</th>
</tr>
</thead>
<tbody>
<tr>
<td>Week 1</td>
<td>Introduction</td>
<td></td>
</tr>
<tr>
<td>Week 2</td>
<td>Economics</td>
<td>Chapter 1/16 (repeatability/correlation/debugging/time to market)</td>
</tr>
<tr>
<td>Week 2</td>
<td>Life of Test Development Engineer</td>
<td></td>
</tr>
<tr>
<td>Week 3</td>
<td>Dies/Packages/Test Boards</td>
<td>Chapter 13</td>
</tr>
<tr>
<td>Week 3</td>
<td>Board Design Consideration</td>
<td>Chapter 13 (gnd/pwr distribution/traces/component/common mistakes)</td>
</tr>
<tr>
<td>Week 3</td>
<td>Device Interface Boards</td>
<td>Chapter 13</td>
</tr>
<tr>
<td></td>
<td>(PCBs/transmission lines/components)</td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>Lab Work – package effects/boards/soldering/fixtures</strong></td>
<td></td>
</tr>
<tr>
<td>Week 4</td>
<td>Introduction to Measurements</td>
<td>Chapter 3</td>
</tr>
<tr>
<td>Week 4</td>
<td>Test Specifications</td>
<td>Chapter 2 (data sheets/test plan/test vectors/test program)</td>
</tr>
<tr>
<td>Week 4</td>
<td>Basic Analog Measurements</td>
<td>Chapter 3 (voltage refs/regulators/impedance meas)</td>
</tr>
<tr>
<td></td>
<td><strong>Lab Work – basic Board Debug</strong></td>
<td></td>
</tr>
<tr>
<td>Week 5</td>
<td>Basic Op Amp Measurements</td>
<td>Chapter 3 (comparator tests/voltage search tech/PSRR/voltage search)</td>
</tr>
<tr>
<td>Week 5</td>
<td><strong>Lab Work – basic Op Amp measurements</strong></td>
<td></td>
</tr>
<tr>
<td>Week 6</td>
<td>Debugging Skills</td>
<td>Chapter 3</td>
</tr>
<tr>
<td>Week 6</td>
<td>Clean-up/Review</td>
<td></td>
</tr>
<tr>
<td><strong>Week 7</strong></td>
<td><strong>Midterm Exam #1</strong></td>
<td></td>
</tr>
<tr>
<td>Week 7</td>
<td>Sampling Theory</td>
<td>Chapter 6 (DSP for aliasing/quantization/jitter/coherency/synchronization)</td>
</tr>
<tr>
<td>Week 8</td>
<td>DSP-Basic IC Testing</td>
<td>Chapter 7</td>
</tr>
<tr>
<td>Week 8</td>
<td>DAC Testing</td>
<td>Chapter 11 (DAC/architectures/basic tests/dynamic tests/common apps tests)</td>
</tr>
<tr>
<td></td>
<td><strong>Lab Work – DAC testing</strong></td>
<td></td>
</tr>
<tr>
<td>Week 9</td>
<td>ADC testing</td>
<td></td>
</tr>
<tr>
<td>Week 9</td>
<td>Basic AC measurements</td>
<td>Chapter 8 (gain/freq/delay/distortion/noise)</td>
</tr>
<tr>
<td></td>
<td><strong>Lab Work – basic AC measurements</strong></td>
<td></td>
</tr>
</tbody>
</table>

*Spring Break*
Week 10  Measurement Errors       Chapter 10  
(tester specs/meas error/data analysis/focused calibration) 

Week 10  Measurement Correction    Chapter 10  
(DC calibrations/AC calibrations/canceling measurement error) 

Week 11  Mixed-Signal Tester Overview    Chapter 5  
(hardware-generic tester architecture/software-LabView/memory)  
Lab Work – references/regulators and accuracy 

Week 12  Digital Testing Overview       Chapter 3  

Week 12  DC/AC Tester Resources       Chapter 5  
(DMM/V&I sources/precision references/calibration)  
(waveform gen/waveform digitizers/time measurement units) 

Week 13  Design for Test (DfT)         Chapter 14  
(BIST/digital, analog, mixed-signal cases) 

Week 13  Review and Synthesize  
Lab Work – clocks & counters 

Week 14  Design Conn 2006 Conference Exhibition 

Week 15  Individual Projects 

May 23rd  FINAL EXAM 12:15 – 2:30pm (In the Lab) 

5. Grades: 

<table>
<thead>
<tr>
<th>Assignment/Lab Work</th>
<th>40%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Midterm</td>
<td>15%</td>
</tr>
<tr>
<td>Class Participation</td>
<td>20%</td>
</tr>
<tr>
<td>Final Exam</td>
<td>25%</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>100%</strong></td>
</tr>
</tbody>
</table>

a. Grading information: curved at the end
b. Extra credit options, if available: by arrangement

c. Penalty (if any) for late or missed work:
   - missed quizzes/exams cannot be made up unless prior arrangements made
   - late work is docked 20% for each day
6. University, College, or Department Policy Information:

a) Academic integrity statement (from Office of Judicial Affairs):
Your own commitment to learning, as evidenced by your enrollment at San José State University &
the University’s Academic Integrity Policy requires you to be honest in all your academic course
work. Faculty is required to report infractions to the Office of Judicial Affairs. The policy on
academic integrity can be found at http://www2.sjsu.edu/senate/S04-12.pdf

b) Campus policy in compliance with the Americans with Disabilities Act:
“If you need course adaptations or accommodations because of a disability, or if you need special
arrangements in case the building must be evacuated, please make an appointment with me as
soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students
with disabilities register with DRC to establish a record of their disability.”

c) Bonus Details: Cell Phones:
Students will turn their cell phones off or put them on vibrate mode while in class. They will not
answer their phones in class. Students whose phones disrupt the course and do not stop when
requested by the instructor will be referred to the Judicial Affairs Officer of the University.

Computer Use:
In the classroom, faculty allows students to use computers only for class-related activities. These
include activities such as taking notes on the lecture underway, following the lecture on Web-based
PowerPoint slides that the instructor has posted, and finding Web sites to which the instructor
directs students at the time of the lecture. Students who use their computers for other activities or
who abuse the equipment in any way, at a minimum, will be asked to leave the class and will lose
participation points for the day, and, at a maximum, will be referred to the Judicial Affairs Officer of
the University for disrupting the course. (Such referral can lead to suspension from the
University.) Students are urged to report to their instructors computer use that they regard as
inappropriate.

Academic Honesty:
Faculty will make every reasonable effort to foster honest academic conduct in their courses. They
will secure examinations and their answers so that students cannot have prior access to them and
proctor examinations to prevent students from copying or exchanging information. They will be on
the alert for plagiarism. Faculty will provide additional information, ideally on the green sheet,
about other unacceptable procedures in class work and examinations. Students who are caught
cheating will be reported to the Judicial Affairs Officer of the University, as prescribed by Academic
Senate Policy S04-12._

7. APPENDIX:
• “In addition to my specifically posted office hours, I am available by arrangement.
• “You are responsible for understanding the policies and procedures about add/drops, academic
renewal, withdrawal, etc. found at http://www2.sjsu.edu/senate/S04-12.pdf
• Expectations about classroom behavior; see Academic Senate Policy S90-5 on Student Rights and
Responsibilities.
• As appropriate to your particular class, a definition of plagiarism, such as that found on Judicial
Affairs website at http://www2.sjsu.edu/senate/plagarismpolicies.htm
• “If you would like to include in your paper any material you have submitted, or plan to submit,
for another class, please note that SJSU’s Academic Integrity policy S04-12 requires approval by
instructors.”
• The name and contact information for the librarian liaison.
• Evacuation plan for the classroom.