San José State University  
Department of Electrical Engineering  
EE 166, Design of CMOS Digital Integrated Circuits,  
Section 01, Spring 2018

Instructor: Sooseok Oh
Office Location: ENG 383, labs (ENG289/291/295)
Email: sooseok.oh@sjsu.edu
Office Hours: Thursday 8:45PM-9:15PM others by appointment
Class Days/Time: TR 7:30PM-8:45PM
Classroom: ENG 238
Prerequisites: EE128 with grade of C or better or instructor’s consent

Course Description
EE166 is an overview of CMOS Integrated Logic Design. Industry standard CAD tools will be used extensively to illustrate principles taught, assignments, and a project.

Course Goals and Student Learning Objectives
1. Prepare students to be productive members of an industrial CMOS digital circuit design team.
2. Prepare students for graduate study or carry out a senior design project in the VLSI field.
3. Provide an understanding of the CMOS logical and physical design
4. Provide an opportunity developing teamwork skills
5. Provide an environment where students learn to think critically
6. Provide an environment where students learn to enjoy the design and learning processes.
7. Have students internalize the culture of the design engineer.

GE/SJSU Studies Learning Outcomes (LO), if applicable
Upon successful completion of this course, students will be able to:

1. GELO 1 Demonstrate an understanding of the fundamentals of Electrical Engineering, including its mathematical and scientific principles, analysis and design.
2. GELO 2 Demonstrate the ability to apply the practice of Engineering in real-world problems.
Course Learning (Outcomes)

To be productive members of an industrial CMOS digital circuit design team, students should be able to:

- analyze circuits using both analytical and CAD tools (k, l)
- use a design flow to design a CMOS integrated circuit in a team environment. (k, l)
- interpret a design specification (c)

To be prepared for graduate study in the VLSI area students should be able to:

- derive basic analytical MOS circuit equations (a)
- locate information not presented in class in the library (i)

Students who can think critically can:

- design test benches that can prove that a design meet a specification (b, e)
- identify regions where circuit models are valid (e)

It is my hope that students learn to enjoy the learning/design process through a “hands on” approach to modern CMOS IC design.

ABET outcomes

The letters in parentheses in the course learning objectives refer to ABET criterion 3 outcomes satisfied by the course. These are listed below as a reference:

(a) An ability to apply knowledge of mathematics, science, and engineering

(b) An ability to design and conduct experiments, as well as to analyze and interpret data

(c) An ability to design a system, component, or process to meet desired needs

(d) An ability to function on multi-disciplinary teams

(e) An ability to identify, formulate, and solve engineering problems

(f) An understanding of professional and ethical responsibility

(g) An ability to communicate effectively

(h) The broad education necessary to understand the impact of engineering solutions in a global and societal context

(i) A recognition of the need for, and an ability to engage in life-long learning

(j) A knowledge of contemporary issues

(k) An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice

(l) Specialization in one or more technical specialties that meet the needs of companies

(m) Knowledge of probability and statistics, including applications to electrical engineering
(n) Knowledge of advanced mathematics, including differential and integral equations, linear algebra, complex variables, and discrete mathematics

(o) Basic sciences, computer science, and engineering sciences necessary to analyze and design complex electrical and electronic devices, software, and systems containing hardware and software components

**Required Texts/Readings**

**Textbook**


**Other Readings**

Other Texts are used as well especially for tri-state logic and clocking. In addition, it can be helpful to read the same material, but from a different perspective to learn difficult concepts. Furthermore, most authors use different examples to drive home concepts.


**Classroom Protocol**

**Cell Phones:**
Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class. Students whose phones disrupt the course and do not stop when requested by the instructor will be referred to the Judicial Affairs Officer of the University.

**Computer Use:**
In the classroom, students are allowed to use computers only for class-related activities. These include activities such as taking notes on the lecture underway, following the lecture on Web-based PowerPoint slides that the instructor has posted, and finding Web sites to which the instructor directs students at the time of the lecture. Students who
use their computers for other activities or who abuse the equipment in any way, at a minimum, will be asked to leave the class and will lose participation points for the day, and, at a maximum, will be referred to the Judicial Affairs Officer of the University for disrupting the course. (Such referral can lead to suspension from the University.) Students are urged to report to their instructors computer use that they regard as inappropriate (i.e., used for activities that are not class related).

**Course Requirements and Assignments**

Class participation, homework, midterm exams, project and final exam Lab experiences will not be graded directly since this course has no associated lab with it. However, the course homework and the project require significant lab time. Plan 10 hours per week as the semester progresses.

**Exams and Grading Policy**

There will be two midterm exams and a final exam. Exams will be closed book. You could bring a calculator and writing instruments to the exam. Programmable calculators are not allowed. There will be no make-up exams (unless under a very special circumstance and when both written excuse and official proofs are provided) and those absent will receive no credit. Late submission of assignments is not accepted for grading.

<table>
<thead>
<tr>
<th>Grades</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Homework</td>
<td>25%</td>
</tr>
<tr>
<td>Midterm Exam1</td>
<td>15%</td>
</tr>
<tr>
<td>Midterm Exam2</td>
<td>15%</td>
</tr>
<tr>
<td>Final Exam</td>
<td>25%</td>
</tr>
<tr>
<td>Project</td>
<td>20%</td>
</tr>
</tbody>
</table>

**Grading Percentage Breakdown**

- 95% - 100%  A
- 91% - 94%   A-
- 87% - 90%   B+
- 83% - 86%   B
- 79% - 82%   B-
- 75% - 78%   C+
- 71% - 74%   C
- 67% - 70%   C-
- 63% - 66%   D+
- 59% - 62%   D
- 55% - 58%   D-
below 54%     F

To support ABET accreditation, and deter violations of academic integrity and the honor code, the instructor keeps a copy of all submitted evaluation instruments of all students. Late work is not accepted and receives zero credit. Please refer to the course schedule for lab, exam, and final evaluation dates and times.
University Policies

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drop, grade forgiveness, etc. Refer to the current semester’s Catalog Policies section at http://info.sjsu.edu/static/catalog/policies.html. Add/drop deadlines can be found on the current academic year calendars document on the Academic Calendars webpage at http://www.sjsu.edu/provost/services/academic_calendars/. The Late Drop Policy is available at http://www.sjsu.edu/aars/policies/latedrops/policy/. Students should be aware of the current deadlines and penalties for dropping classes.

Information about the latest changes and news is available at the Advising Hub at http://www.sjsu.edu/advising/.

Academic integrity

Your commitment, as a student, to learning is evidenced by your enrollment at San Jose State University. The University Academic Integrity Policy S07-2 at http://www.sjsu.edu/senate/docs/S07-2.pdf requires you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The Student Conduct and Ethical Development website is available at http://www.sjsu.edu/studentconduct/.

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person’s ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that University Policy S12-7, http://www.sjsu.edu/senate/docs/S12-7.pdf, requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 at http://www.sjsu.edu/president/docs/directives/PD_1997-03.pdf requires that students with disabilities requesting accommodations must register with the Accessible Education Center (AEC) at http://www.sjsu.edu/aec to establish a record of their disability.

Accommodation to Students' Religious Holidays

San José State University shall provide accommodation on any graded class work or activities for students wishing to observe religious holidays when such observances require students to be absent from class. It is the responsibility of the student to inform the instructor, in writing, about such holidays before the add deadline at the start of each semester. If such holidays occur before the add deadline, the student must notify the instructor, in writing, at least three days before the date that he/she will be absent. It is the responsibility of the instructor to make every reasonable effort to honor the student request without penalty, and of the student to make up the work missed. See University Policy S14-7 at http://www.sjsu.edu/senate/docs/S14-7.pdf.
## Tentative Course Schedule

<table>
<thead>
<tr>
<th>Date</th>
<th>Topic</th>
<th>Readings and assignments</th>
</tr>
</thead>
<tbody>
<tr>
<td>01/25/2018</td>
<td>Introduction and overview</td>
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</tr>
<tr>
<td>01/30/2018</td>
<td>CMOS Transistor</td>
<td>HW1</td>
</tr>
<tr>
<td>02/01/2018</td>
<td>CMOS Transistor</td>
<td></td>
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<tr>
<td>02/06/2018</td>
<td>Lab day</td>
<td>Review of CAD tools</td>
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<tr>
<td>02/08/2018</td>
<td>Boolean logic review</td>
<td>HW2</td>
</tr>
<tr>
<td>02/13/2018</td>
<td>CMOS Logics</td>
<td>Project group discussion</td>
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<tr>
<td>02/15/2018</td>
<td>Combinational Logics</td>
<td>HW3</td>
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<tr>
<td>02/20/2018</td>
<td>CMOS Delay</td>
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<tr>
<td>02/22/2018</td>
<td>CMOS Delay</td>
<td>HW4</td>
</tr>
<tr>
<td>02/27/2018</td>
<td>Midterm Review</td>
<td></td>
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<tr>
<td>03/01/2018</td>
<td>Midterm #1</td>
<td></td>
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<tr>
<td>03/06/2018</td>
<td>Physical Design</td>
<td>HW5, Project discussion</td>
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<tr>
<td>03/08/2018</td>
<td>CMOS latch/flip-flop</td>
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<tr>
<td>03/13/2018</td>
<td>Timing analysis</td>
<td>HW6</td>
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<tr>
<td>03/15/2018</td>
<td>Physical design planning</td>
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<tr>
<td>03/20/2018</td>
<td>Sequential logics</td>
<td>HW7</td>
</tr>
<tr>
<td>03/22/2018</td>
<td>Sequential logics</td>
<td></td>
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<tr>
<td><strong>03/27/2018</strong></td>
<td><strong>Spring Recess</strong></td>
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<tr>
<td><strong>03/29/2018</strong></td>
<td><strong>Spring Recess</strong></td>
<td></td>
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<tr>
<td>04/03/2018</td>
<td>Midterm review</td>
<td></td>
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<tr>
<td>04/05/2018</td>
<td>Midterm #2</td>
<td></td>
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<tr>
<td>04/10/2018</td>
<td>Adders</td>
<td>HW8</td>
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<tr>
<td>04/12/2018</td>
<td>Shifters</td>
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<tr>
<td>04/17/2018</td>
<td>Pass logics</td>
<td>HW9</td>
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<tr>
<td>04/19/2018</td>
<td>Timing of complex circuits</td>
<td></td>
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<tr>
<td>04/24/2018</td>
<td>Low power design technique</td>
<td>HW10</td>
</tr>
<tr>
<td>04/26/2018</td>
<td>Modern SOC design</td>
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<tr>
<td>05/01/2018</td>
<td>Embedded system design</td>
<td></td>
</tr>
<tr>
<td>05/03/2018</td>
<td>Project report due</td>
<td>Final project review</td>
</tr>
<tr>
<td>05/08/2018</td>
<td>Review of course</td>
<td></td>
</tr>
<tr>
<td>05/10/2018</td>
<td>Last Class</td>
<td>Last day of class</td>
</tr>
<tr>
<td>05/17/2018</td>
<td>Final Exam</td>
<td>19:45-22:00</td>
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</tbody>
</table>
EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

“I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- Take an exam in place of someone else, or have someone take an exam in my place
- Give information or receive information from another person during an exam
- Use more reference material during an exam than is allowed by the instructor
- Obtain a copy of an exam prior to the time it is given
- Alter an exam after it has been graded and then return it to the instructor for re-grading
- Leave the exam room without returning the exam to the instructor.”

Measures Dealing with Occurrences of Cheating

- Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.
- A student’s second offense in any course will result in a Department recommendation of suspension from the University.

Professional Attitude

- In addition to the honor code, students understand that a professional attitude is necessary to maintain a comfortable academic environment.
- Come to the lectures on time and remain for the entire duration of the session
- Do not talk to friends during class.
- To minimize possible tension during exams, follow the exam rules closely