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Design of a Ultra-Low Power 10-bit Successive Approximation ADC in 45nm CMOS Technology

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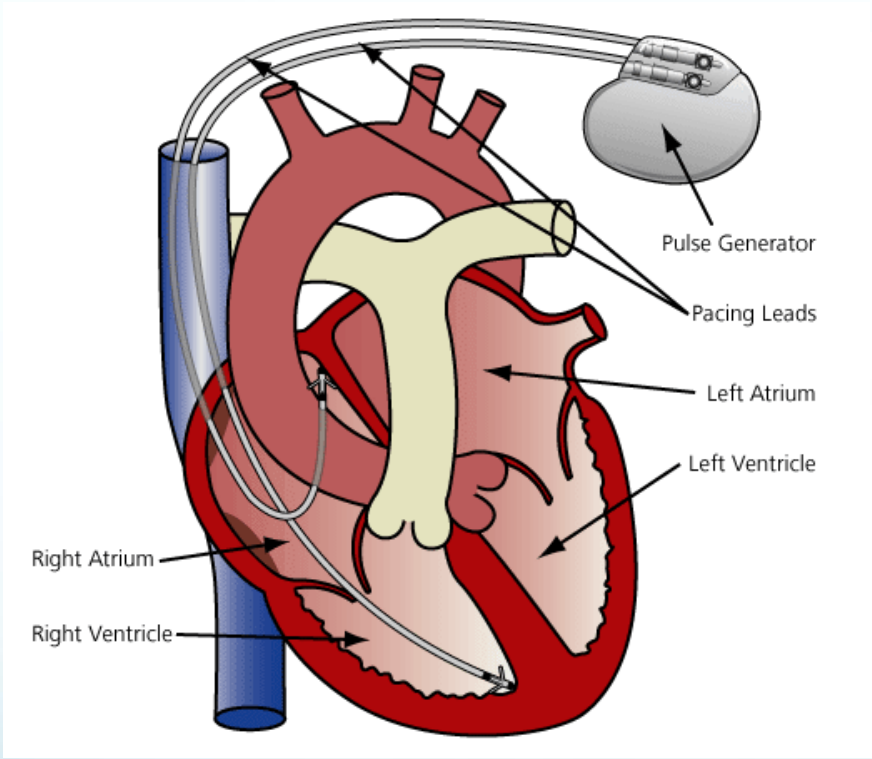
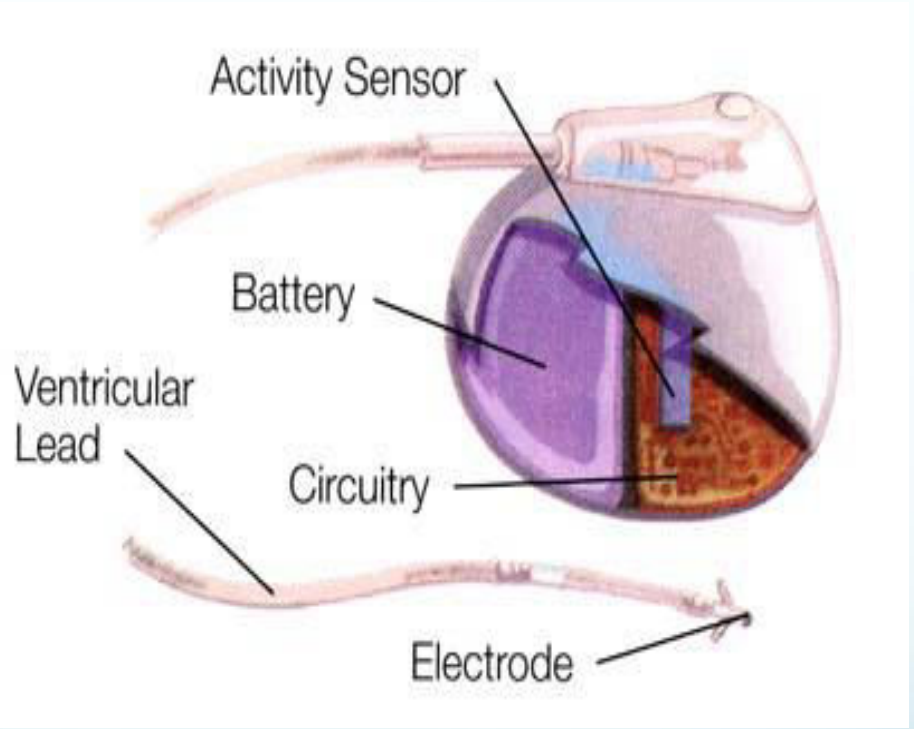
Overview

- **Implantable Cardiac Pacemaker**
- **Charge Redistribution SAR Architecture**
- **Binary Weighted Capacitive DAC**
- **Two-Stage Dynamic Latch Comparator**
- **Synchronous Logics**
- **Power Consumption**
- **ADC Performance**
- **Comparison**

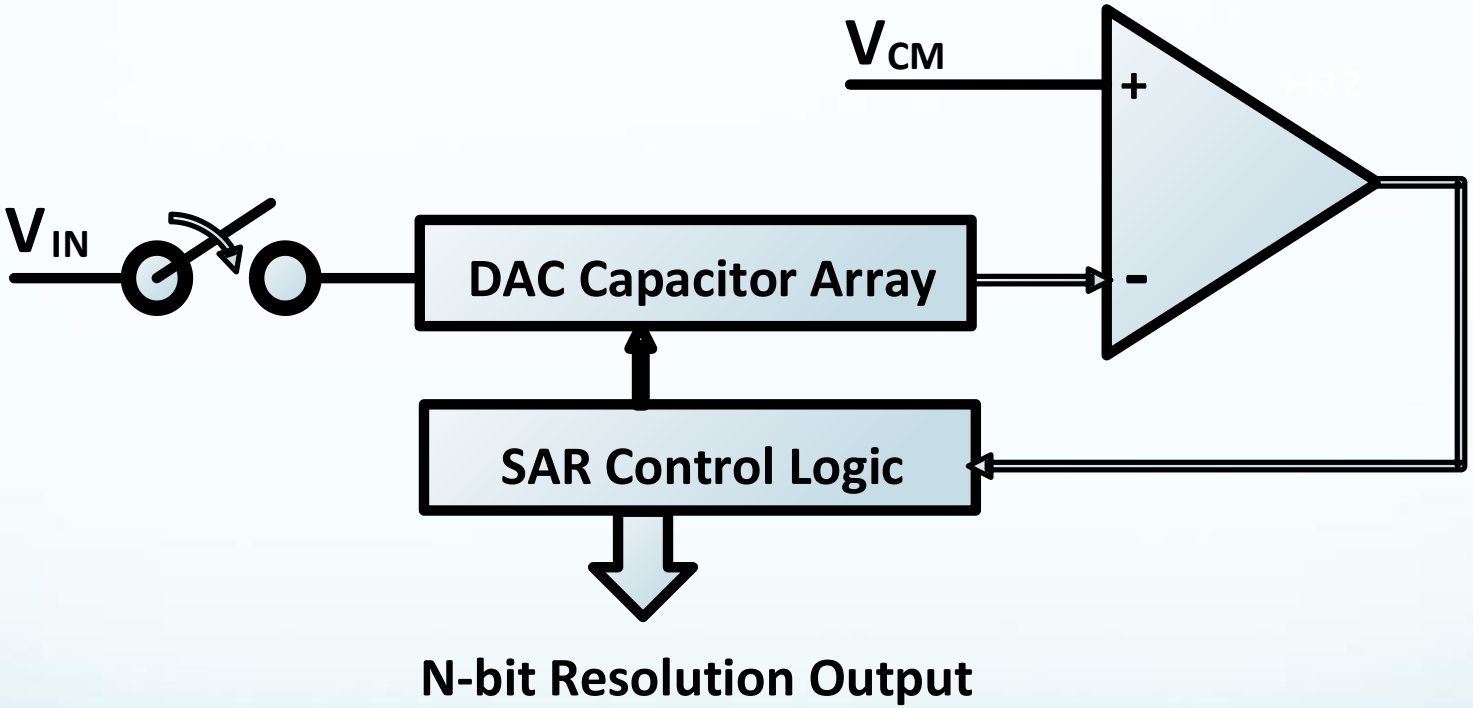
Implantable Cardiac Pacemaker





[1] L. S. Y. Wong, S. Hossain, A. Ta, J. Edvinsson, D. H. Rivas, and H. Nääs. “A Very Low-Power CMOS Mixed-Signal IC for Implantable Pacemaker Application,” ISSC,2004.

Charge Redistribution SAR Architecture

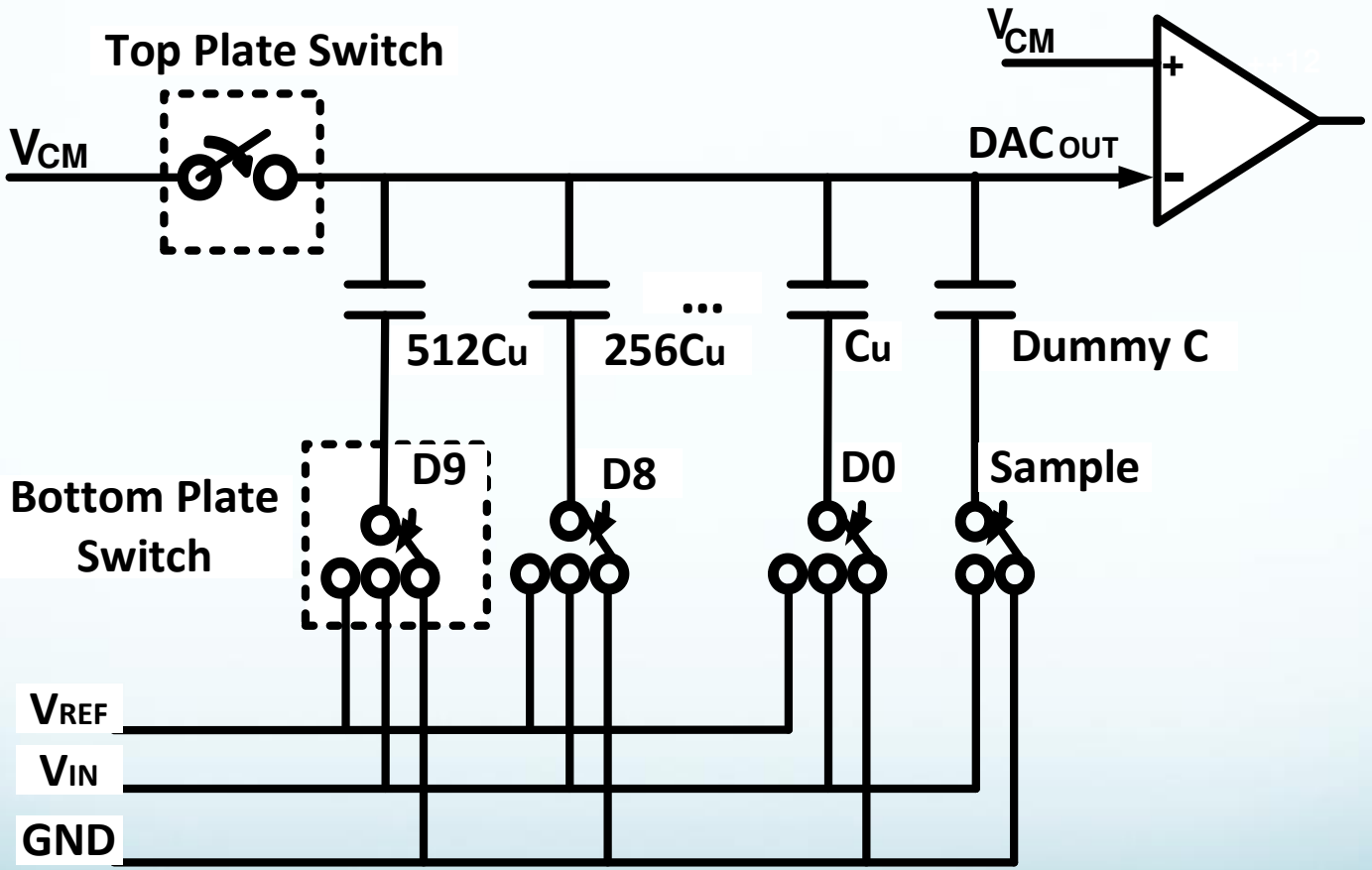


[2] J. L. Mccreary and P. R. Gray, “All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques – Part 1,” *ISSC*, vol. sc-10, no. 6, Dec., 1975.

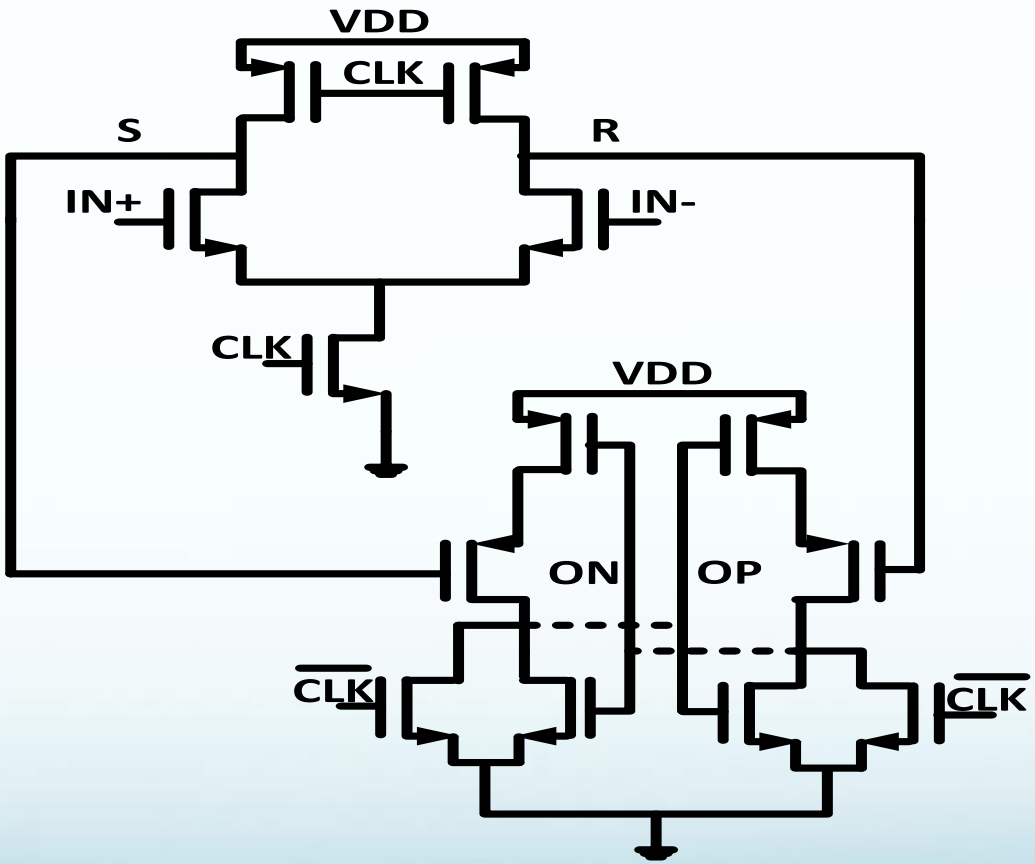
Specification

- **10-bit Resolution**
- **1.2V Supply Voltage**
- **Sampling Frequency <10MS/s**
- **Ultra-Low Power**
- **Small Area**
- **45nm CMOS Technology**

Binary Weighted Capacitive DAC

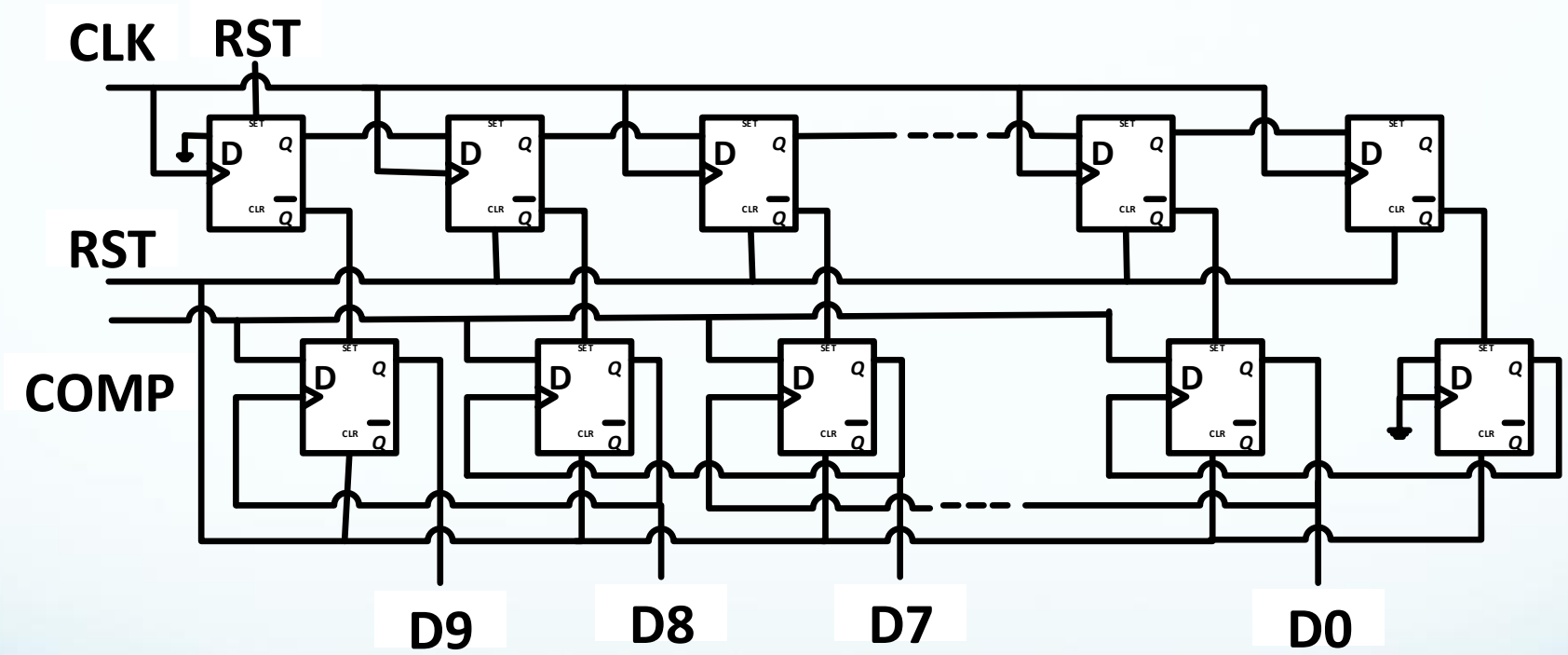


Two-Stage Dynamic Latch Comparator



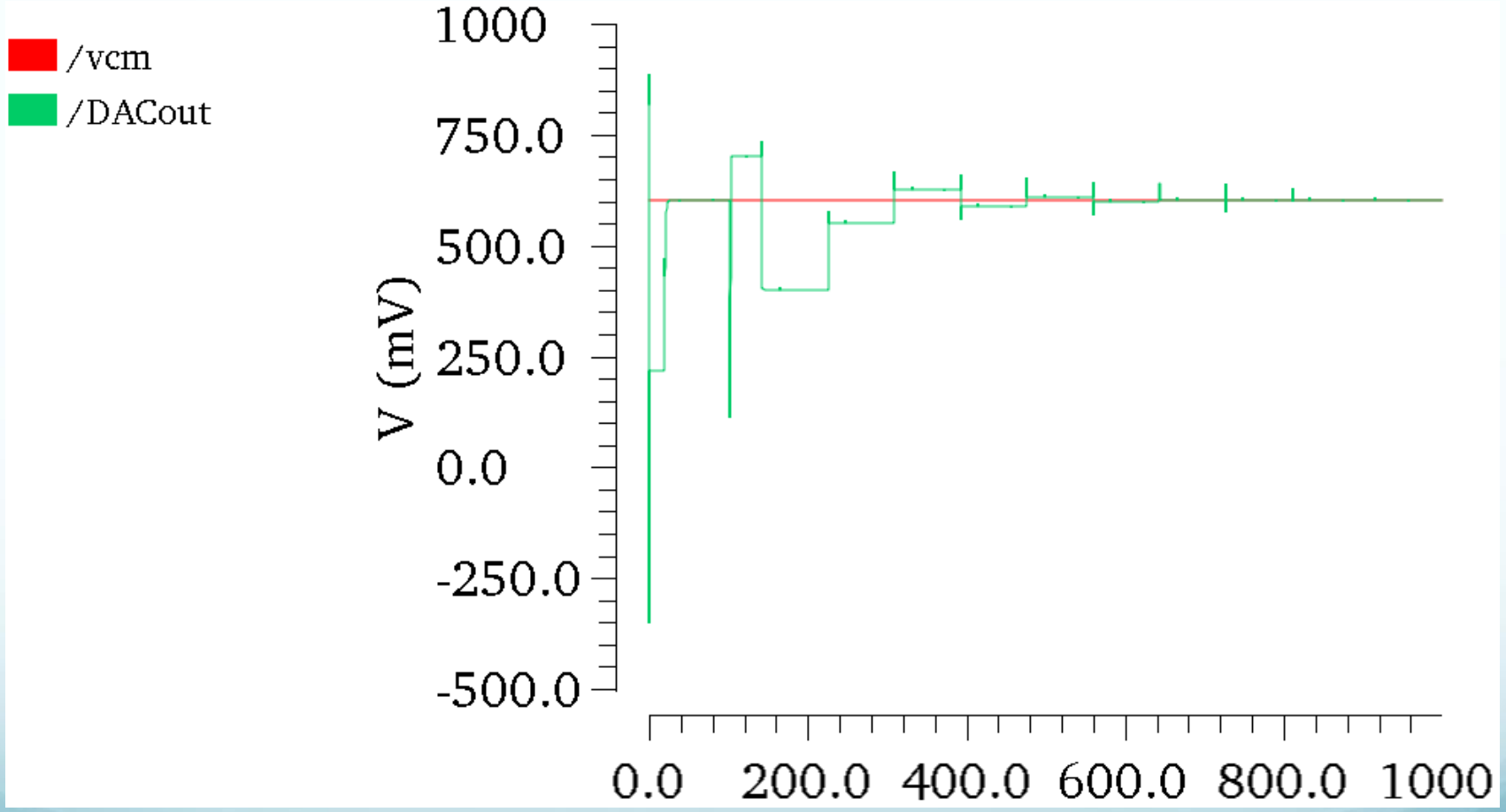
[3] Michiel van Elzakker, E. Tuijl, P. Geraedts, D. Schinkel, E. A. M. Klumperink, and B. Nauta, “A 10-bit Charge-Redistribution ADC Consuming1.9μW at 1 MS/s,” ISSC, 2010.

Synchronous Logics



[4] M. D. Scott, B. E. Boser and K. S. J. Pister, “An Ultralow-Energy ADC for Smart Dust,” *IEEE Journal of Solid-State Circuits*, vol. 38, no. 7, July, 2003.

DAC Output


/vcm
/DACout
1000
750.0
500.0
250.0
0.0
-250.0
-500.0
V (mV)
0.0
200.0
400.0
600.0
800.0
1000

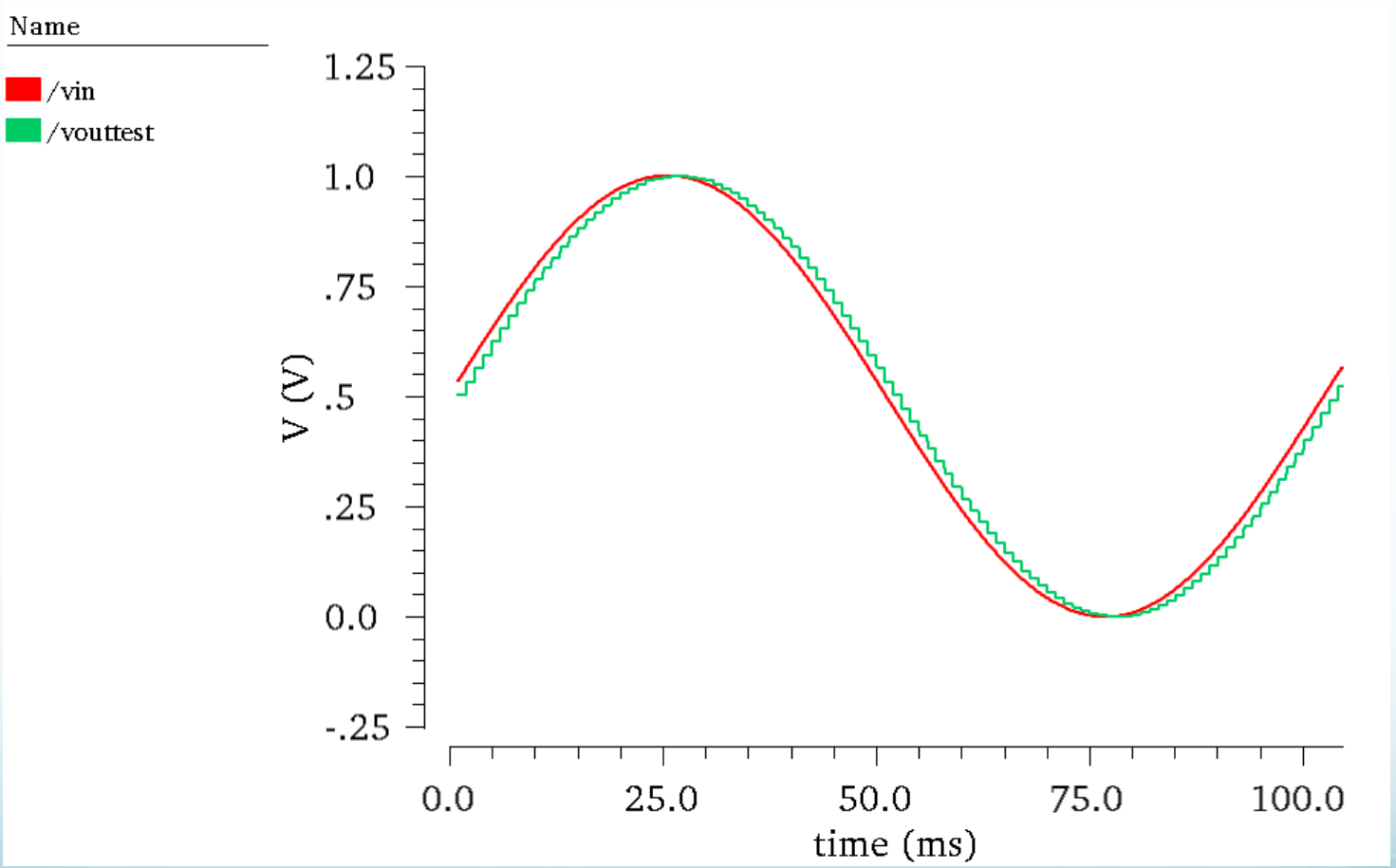
ADC Outputs

Inout\ Output	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1.2v	1	1	1	1	1	1	1	1	1	0
1.1v	1	1	1	0	1	0	1	0	1	0
1v	1	1	0	1	0	1	0	1	0	1
900mv	1	1	0	0	0	0	0	0	0	0
800mv	1	0	1	0	1	0	1	0	1	1
700mv	1	0	0	1	0	1	0	1	0	1
600mv	1	0	0	0	0	0	0	0	0	1
500mv	0	1	1	0	1	0	1	0	1	1
400mv	0	1	0	1	0	1	0	1	1	0
300mv	0	1	0	0	0	0	0	0	0	1
200mv	0	0	1	0	1	0	1	0	1	1
100mv	0	0	0	1	0	1	0	1	1	0
0v	0	0	0	0	0	0	0	0	0	1

Power Consumption

Block	27℃	70℃	85℃	100℃	Unit
SAR Logic	18.63	36.87	46.86	59.36	nW
DAC	5.02	11.06	14.26	18.24	nW
Comparator	1.93	4.44	5.76	7.33	nW
Total	25.58	52.37	66.88	84.93	nW

ADC Test for ENOB/SFDR



ADC Performance

Performance	Result	Unit
Process Technology	45nm	
Supply Voltage	1.2	V
Resolution	10	bits
Sampling Frequency	1	kS/s
Power Consumption	25.58	nW
SINAD	61.75	dB
SFDR	66.52	dB
ENOB	9.96	bits
FoM	25.68	fJ/conversion-step

Performance Comparison

Performance	This work	[3]	[4]	[5]	[6]
Process Technology	45nm	90nm	65nm	0.18um	0.25 um
Supply Voltage (V)	1.2	1	1	1	1
Resolution (bit)	10	9	10	9	8
Sampling Frequency (S/s)	1K	20M	1M	150K	100K
Power Consumption (W)	25.58n	290u	1.9u	30u	3.1u
ENOB (bit)	9.96	7.8	8.75	8.2	7.9
FoM (fJ/conversion-step)	25.68	65	4.4	680	130

Conclusion

- **Excellent Performance**
- **ENOB of 9.96 bit**
- **Ultra-Low Power Consumption of 25.58nW**
- **Energy efficiency of 25.68fJ/conversion**


Q&A

References

- [1] L. Wong, S. Hossain, A. Ta, J. Edvinsson, D. Rivas, and H. Nääs. "A Very Low-Power CMOS Mixed-Signal IC for Implantable Pacemaker Application,"*IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, Dec 2004.

- [2] J. L. Mccreary and P. R. Gray, "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques – Part 1," *ISSC*, vol. sc-10, no. 6, Dec., 1975.

- [3] Michiel van Elzakker, E. Tuijl, P. Geraedts, D. Schinkel, E. A. M. Klumperink, and B. Nauta, "A 10-bit Charge-Redistribution ADC Consuming1.9μW at 1 MS/s," *IEEE J. Solid-State Circuits*, VOL. 45, NO. 5, MAY 2010.

- [4] M. D. Scott, B. E. Boser and K. S. J. Pister, "An Ultralow-Energy ADC for Smart Dust," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 7, July, 2003.

- [5] J. Sauerbrey, D. Schmitt-Landsiedel, and R. Thewes, "A 0.5-v 1-μW Successive Approximation ADC," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 7, July 2003.

- [6] J. Cranninckx and G. Van der Plas, "A 65fJ/conversion-step 0-to-50MS/s 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS," *ISSCC Dig.Tech.Papers,* Feb. 2007.

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