Implementation of a DDR3 SDRAM Memory Subsystem on a Xilinx 7-Series FPGA with ARM AXI4 and DFI

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Summary

DDDR3 SDRAM is the one of the most ubiquitous memory technology used in the electronics industry. It is utilized in high-end embedded applications, tablets, laptop computers, desktop computers, servers, etc. It is also widely used in conjunction with FPGA hardware-based applications. While there have been many FPGA vendor supplied DDR3 SDRAM controller and PHY solutions, most solutions rely on a proprietary interface between the DRAM controller and PHY. This has created a situation where the designer is locked to a particular FPGA vendor's device. We have created an industry standard-based DDR3 SDRAM PHY for Xilinx 7 series FPGA utilizing DFI (DDR PHY Interface). DFI is a standardized interface widely used in ASIC design to connect a DDRx SDRAM controller to a DDR interface PHY. To verify the functionality of our DFI PHY, we also developed a DDR3 SDRAM controller with ARM AMBA 4 AXI4 protocol and an AXI4 protocol traffic generation verification vehicle.

Design Goal

In order to design a high-performance and flexible DDR3 SDRAM subsystem, this project started off the design process with the following goals.

- Adoption of industry standard such as ARM AMBA (Advanced Microcontroller Bus Architecture) and DFI (DDR PHY Interface) to facilitate an SoC (System on a Chip) centric design methodology.
- Separation and encapsulation of device vendor specific components such as PLL (Phase Locked Loop), RAM, and I/O FF, and I/O pad in order to facilitate modular design philosophy.
- Parameterization of design parameters such as address, data, and counter widths in the Verilog RTL (Register Transfer Level) code.
- Externally adjustable parameters in order to make the design capable of targeting different operating conditions such as being able to alter memory capacity or timings without a major design respin.
- Package the resulting design as a reusable design in order to explore an IP (Intellectual Property) core licensing business model as a way to market the design.

DDR3 SDRAM Memory Sub-System

 AXI4 Traffic Generator

- 64-bit wide DDR3 SDRAM interface
- Supports x8 and x16 with DFI AXI4 Interface
- Up to 2 rank support (at this time, only 1 rank configuration is supported)
- 128-bit wide DFI data path with 1:1 frequency ratio
- Performs write leveling, read gate training, and read training at initialization and during run time
- Periodic read data eye calibration with minimal performance impact
- Internally utilizes Xilinx specific components such as IDDR, ODDR, IDELAY2, ODELAY2 (hidden from outside)

 Primary References

- Mentor Technology, Incorporated, DDR3 SDRAM 10x4, x8, x16, 2006
- Brece Design Solutions, SDRAM Controller IP Core (Prototype).

Design Environment

- Xilinx: XST 14.7 Evaluation Kit (Xilinx Artix 7 FPGA, ZCY70117TFFG676-2)
- Xilinx Vivado Logic Analyzer (Integrated LogicAnalyzer for debugging and validation use)

Potential Future Enhancements

- The entire design is portable to other platforms such as Xilinx UltraScale system Calibration for High Performance DDR Interface IP, Synopsys User Group, 2010
- External utilization of Xilinx IDDR, ODDR, IDELAY2, ODELAY2 (hidden from outside)

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Memory Controller

- 128-bit wide DFI data path with 1:1 frequency ratio
- Supports all 1 Gb to 8 Gb density x8 and x16 with DFI devices
- DFI timing parameters such as C1, (CAS Latency), RCD, DQ, RAS, etc., refresh interval, row size, column size, and address mapping from the DRAM are configurable via the DFI (Parameter Setting) module.
- Up to 2 ranks support (2 rank support is implemented internally)
- ARM AMBA 4 (Advanced Microcontroller Bus Architecture 4) AXI4 (Advanced eXtensible Interface 4) protocol with 256-bit wide data path, 36-bit address field, and 4-bit wide ID
- AXI4 protocol runs at ½ of native clock frequency of DFI MAC
- Automatic per bank row management with up to 8 open rows per rank
- Automatic refresh command issuance
- 8 entry FIFO buffer for Write Address Channel, Read Address Channel, Write Data Channel, and Read Data Channel
- Completion of Verilog RTL code for maximum design portability with RAM component encapsulation

Primary References

- Mentor Technology, Incorporated, DDR3 SDRAM 10x4, x8, x16, 2006
- Brice Design Solutions, SDRAM Controller IP Core (Prototype).