Design and Performance Analysis of Real Time Optical Flow Computation on FPGA

Dr. Chang “Charles” Choo, Vrishbhan Singh Sisodia, Virendra Kate
Department of Electrical Engineering, San Jose State University, San Jose, California 95192

Introduction

One of the important aspects of the driverless car is analyzing the changes in the surroundings for a safe and comfortable ride. Our project aims at designing an FPGA based system that computes optical flow of surrounding objects and mapping the movement to show the movement in the two successive video frames in real time.

This project has three major sections;
• FAST corner detection,
• motion estimation using Sum of Absolute Difference (SAD) based block matching algorithm,
• implementing the algorithm that integrates the two algorithms for optical flow computation.

This poster discusses about the implementation, results and performance analysis of FAST algorithm

Features from Accelerated Segment Test (FAST) Algorithm
• In a segment test, the pixel of interest is compared locally with surrounding pixels (Circular region)
• p is classified as a corner if there exists a set of n contiguous pixels in the circle which are all brighter than p by more than threshold value.
• the test examines only the four pixels at 1, 5, 9 and 13 (the four compass directions). If p is a corner then at least three of these must all be brighter than I<sub>p</sub> + t or darker than I<sub>p</sub> - t [3]

The highlighted squares are the pixels used in corner detection. The pixel p is the center of the candidate pixel. The arc is indicated by the dashed line and passes through 12 contiguous pixels which are brighter than p by more than threshold value.

Results from real time FAST corner detection. The analysis was performed on Zyng xc702 SoC board at 150MHz and the video input was processed at 60fps. The total LUT utilization was approximately 20K which accounted for around 40% of the total available resources.

The corners detected will be later used to select the blocks in the image which will be used for SAD based block matching for motion estimation of the objects.

Design Approach

Key steps for corner detection using FAST algorithm:
• Step 1: Capture video
• Step 2: Convert video into frames
• Step 3: Convert video frame from color to grayscale
• Step 4: Store incoming pixel stream into the line buffers for video frames
• Step 5: Sliding window selects data from line buffers which is used for calculations
• Step 6: FAST corner detection performed
• Step 7: Mask is created based on FAST calculation
• Step 8: Mask is superimposed on the current frame
• Step 9: Video is created back from the superimposed frames

Implementation Results -

The LUT utilization varies with the width of the image and for the same width the utilization remains the same. Among different FPGA families Zyng has the least LUT utilization but as a trade off uses max number of Flip-Flops.

Latency Comparison

Latency varies with the height of the image, the higher the more is the latency. Among different FPGAs the Virtex 7 family is slightly faster.

Conclusions

This project presented and successfully implemented a different and unique approach to compute the optical flow by integrating FAST corner algorithm and the Sum of Absolute Differences (SAD) based motion estimation algorithm in a cost effective way on Xilinx Zyng xc702 FPGA for a real time application. This design, due to its cost effectiveness enables other modules to use the available system resources. The calculated optical flow results can further be used to find the relative velocities of the objects in an environment.

Key References

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For further information

Please contact vrishbhansingh.sisodia@sjsu.edu or virendra.kate@sjsu.edu