StrongARM based Time to Digital Converter

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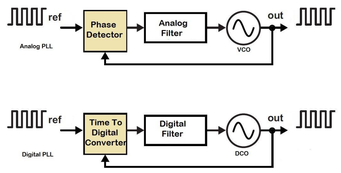
Introduction

There is an ever increasing demand for faster, accurate and more robust high speed data transmission links to exchange information across huge distances via various channels. Signal processing forms the core of data transmissions and Analog and Mixed Signal blocks (AMS) especially the (Phase Locked Loops PLL) constitute the crux of these transmission blocks. This increased need demanded scaling down the basic building elements to Nano-scale CMOS technology fabrication regime, which is already challenged by the complex architectures giving raise to increased parasitic effects and decreased gain. Reduced signal swing is the prominent reason for decreased Signal to Noise Ratio (SNR) at high speeds.



Analog and Digital implementation of PLL is shown in the figure above. The distinct block between the architectures is the error detection part. This error detecting block is called the Phase Detector. This phase detector is can be implemented in digital way by block called Time to Digital Converter (TDC) where the difference in the arrival time of the two signals is be measured and this information in form of logic values or bits is fed to proceeding blocks [1].

Methodology

TDC Working Principle

The basic principle of operation of a Time-to-digital converter is first to change the time difference between the signals under test into a voltage levels and then to convert these voltage level to binary or gray code for feeding information to the next stage.

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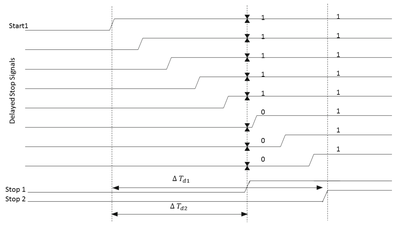


Considering an N stage network with a constant equal interim delay maintained at T_R's can represent a maximum of T_D's as a thermometer code whose relation is shown in Eq. 1.

$$T_D = N \cdot T_R \qquad 1.$$

Methodology

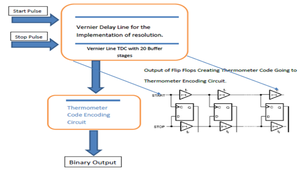
State of the Art : Delay Line

1. Vernier Delay Line

In general Vernier delay line is time stretching method where the two signals under considerations are delayed by unequal values. So in time, the less delayed signal catches up with the more delayed signal.

Consider two buffer stages as shown in the Figure 5; by definition of Vernier delay chain the delay of the buffer in top chain is greater than the delay of the buffers in lower chain. Thus making the $T_{Upper\ Delay} > T_{Lower\ Delay}$.

$T_{Vernier,res} = T_{upper\ delay} - T_{Lower\ delay}$ 2.



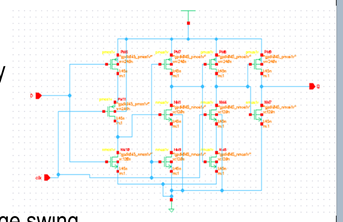
Therefore the resolution given by Eq.2 is dependent on the difference of two delay stages instead of one delay element. This ensures that for good value of resolution and stages we can achieve better dynamic range.

State of the Art : Flip Flops

2. TSPC [2]

Advantages:

- Fast Clock to Q delay
- Works on Dynamic Logic principle.

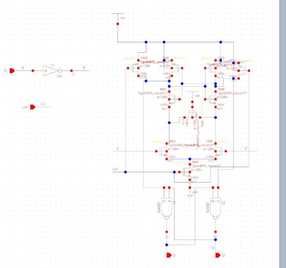


Challenges:

Reduced output voltage swing

If clock rise time is large, hold time violations occur.

3. StrongARM Latch [3



Two stages implemented

3.1 Clocked comparator

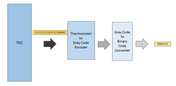
3.2 RS Latch

Advantages:

- Design ensures no Static power
- Full Rail to rail swing
- Input transistors are sized to have minimal delay and no timing violations

3. State of the Art : Encoder

Combinational Thermometer to Binary converter is realized in 45nm CMOS. Here first the thermometer code is converted to gray code and then to Converted to binary code. The advantage of this intermediate conversion minimizes bubble errors.[4]

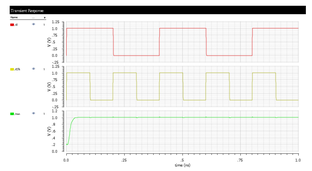


Results

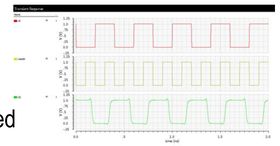
Simulation Results:

TSPC Flip Flop

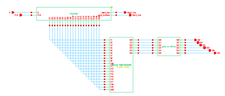
Failed at 200ps clock due to hold time violations, shows the challenges, but appropriate sizing ensured correct behavior.

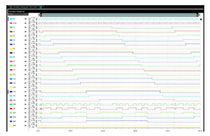


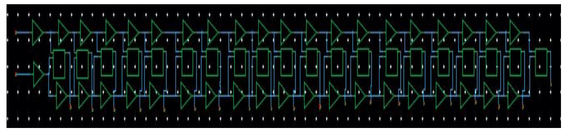
The figure besides shows the StorngARM latch locked at 5 GHz clock and 2.5 GHz data. input transistors were decreased in size to reduce the

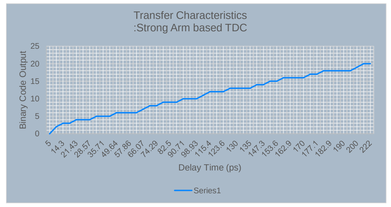


The figure beside shows the test bench setup for both TSPC and Strong ARM FF and the corresponding sampled thermometer code output along with binary encoded output data. Below shows the schematic capture of the 20 stage delay line based TDC with flip flops for sampling.

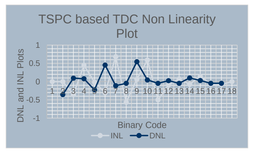


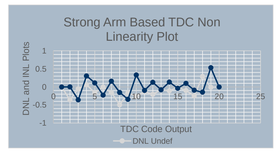






StrongARM based TDC Transfer Characteristics simulated for a dynamic range of 220ps. The Above Figure show The DC characteristics shows the TDC behavior as a linear phase detector.





From the transfer curves plotted under plots we calculate the Non-linearity plots of the each topology .

The DNL/INL of TSPC is around +0.45/+0.682 and the corresponding values for StrongARM based TDC was calculated to be +0.29/+0.53. The Max INL and DNL of $\mathrm{TSPC} > \mathrm{StongARM}$, this shows that the latter topology is more robust towards minor variation in the delay chain.

Summary

A Time-to-Digital Converter is designed and simulated using two different topologies with TSPC Flip Flop and StrongARM latch. All the designs are calculations are for 45nm technology. . TSPC Flip Flop posed critical challenges if the rise time of clock is large causing hold time violation. This makes it un reliable for a higher number of stages.

On the other hand StrongARM latch showed significant stability and robust performance due its operating region and stable structure, Higher number of stages and more resolution be achieved

Key References

[1] R. B. Staszewksi, vLeipold D, M. K and P. T. Balsara, "Digitally controlled oscillator (DCO)- Based architecture for RF frequency synthesis in a deep-submircormeter CMOS process," IEEE Trans. Circuits Syst. II.,, pp. 815-828, 2003.

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[3] K. Jaeha, L. B S, R. Jihong and M. C J, "Simulation and Analysis of Random Decision Erros in Clocked Comparators," Circuits and Systems I, IEEE Transactions on, pp. 1844,1857, 2009.

[4] S. Sheikhaei, S. Mirabbasi and I. A, "An encoder for a 5GS/s 4 bit-flash ADC in 0.18/spl mu/m CMOS," in Canadian Conference on Electrical and Computer Engineering, IEEE, 2005.

Acknowledgements

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