Design of an Ultra-Low Power 10-Bit Successive Approximation ADC

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Introduction

In recent years, there has been increasing demand for Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs) for a range of low power medical implant devices like the cardiac pacemaker illustrated in Figure 1, which can detect and control the speed and pattern of the human heartbeat [1].

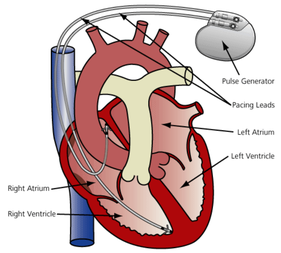


Figure 1 Cardiac pacemaker [1]

The ADC as a critical component in the input block of the implantable cardiac pacemaker consumes a high amount of power by digitizing the amplified sensed signal. As such, the critical need for long battery lifetime in implantable pacemakers has motivated the demand for designing low power SAR ADCs. A 10-bit ultra-low power SAR ADC for the first time is designed in a 45nm CMOS technology. This unique ADC with sampling frequency of 1kS/s at supply voltage of 1.2V consumes total power of 25.58nW and achieves an energy efficiency of 25.68fJ/conversion. An Effective Number of Bits (ENOB) of 9.96 bits is obtained.

Methodology

SAR ADC Architecture

The 10-bit SAR ADC is designed based on the charge redistribution architecture shown in Figure 2. It consists a capacitive DAC with inherent sample-and-hold circuit, a two-stage dynamic latch comparator and , a digital SAR logic.

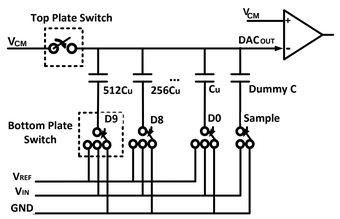


Figure 2 10-bit SAR ADC architecture [2]

Digital to Analog Converter

The 10-bit Digital to Analog converter is applied with a binary weighted capacitor array on the basis of the charge redistribution architecture as illustrated in Figure 2. A pair of different switch blocks are utilized to control manage the voltage paths including input voltage (V_{in}), reference voltage (V_{ref}), ground and common mode voltage (Vcm) that is used instead of the ground in Figure 2, to bottom and top plates of the array.

Methodology

DAC normally suffers from the capacitor mismatch due to the process variation. Thus, the value of the unit capacitance should be as small as possible to reduce the power consumption. The minimum value of the unit capacitor is limited by several factors including thermal noise, capacitor matching and the value of the parasitic capacitances [3]. The rest of capacitors in array are sized with a binary weighted value of the unit capacitor. There are two sets of top and bottom plate switches designed to perform the sampling in DAC.

Comparator

Although the latch-only comparators offers low power and fast speed, they tend to have high kickback noise and input offset error. Therefore, to mitigate these issues energy efficient two-stage dynamic latch comparator shown in Figure 3 designed. The first stage is a voltage amplifier and a latch is the second stage.

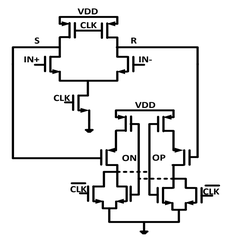


Figure 3 Two-stage dynamic latch comparator [4]

Successive Approximation Register

The synchronous successive approximation register (SAR) illustrated in Figure 4 is chosen for this project. It is based on sequencer (ring counter) and code register that includes 2N+2 Flip-Flops (FF) to control a DAC, while N+1 Flip flops are for the code register and N+1 FF for the sequencer. The upper Flip-Flop row is a sequencer or shift register. The lower row is a code register.

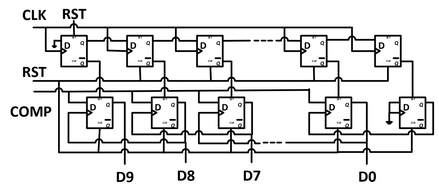
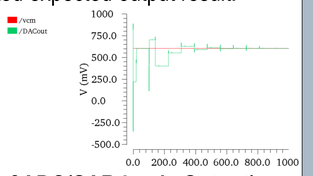


Figure 4 Synchronous SAR Logic [5]

Results

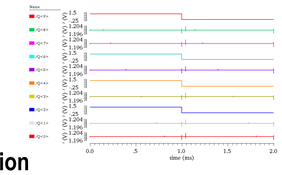
Evaluation of Functionality of ADC (DAC Output)

A simulation performed to confirm the operation of the ADC. A 500mV constant input signal is sent to the ADC. Then, output of the DAC is monitored. A DAC output waveform (Figure 5) eventually reaches the common mode voltage V_{CM} and the waveforms match the calculated expected output result.



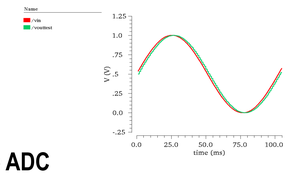
Evaluation of Functionality of ADC(SAR Logic Output)

ADC simulated to justify the operation. The ADC tested under the input voltage of 500mV, 1.2V supply voltage, 12 kHz clock frequency, and temperature of 27ºC. The output data as expected (0110101011) illustrated below.



SINAD/SFDR/ENOB Evaluation

The Fast Fourier Transform (FFT) can achieve the dynamic performance of the ADC including SINAD, SFDR and ENOB. Input and reconstructed output waveforms of the ADC shown below. A 10Hz sine wave is applied to the ADC and the output data is recorded. The simulation results of measured FFT spectrum at 10 Hz input signal frequency achieved 9.4 of ENOB as a result of the SINAD equal to 58.41. SFDR of the ADC according to FFT spectrums is 63.18.



Power consumption of the ADC

All the power consumption of a SAR ADC is measured in cadence virtuoso under the analog sine wave input with 500 Hz frequency, 1.2V supply voltage, for the range of temperatures range between 27ºC to 100ºC . Table 1 shows the power consumption of each block and the total power consumption of the SAR ADC.

Table 1 The ADC blocks power consumption

SAR ADC Block	Power Consumption at 27°C	Power Consumption at 70°C	Power Consumption at 85°C	Power Consumption at 100°C	Unit
SAR Logic	18.63	36.87	46.86	59.36	nW
DAC	5.02	11.06	14.26	18.24	nW
Comparator	1.93	4.44	5.76	7.33	nW
Total	25.58	52.37	66.88	84.93	nW

The performance of ultra-low SAR ADC is provided in Table 2.

Table 2 Ultra-low SAR ADC Performance

Performance	Result	Unit
Process Technology	45nm	
Supply Voltage	1.2	v
Resolution	10	bits
Sampling Frequency	1	kS/s
Power Consumption	25.58	nW
SINAD	61.75	dB
SFDR	66.52	dB
ENOB	9.96	bits
FoM	25.68	fJ/conversion-step

Summary

A 10-bit successive approximation register (SAR) analog to digital converter (ADC) successfully designed with 1kS/s sampling frequency and supply voltage of 1.2 V in 45nm CMOS technologyThe ADC employs a charge-redistribution DAC with inherent sample and hold circuit, a two-stage dynamic comparator, and a synchronous SAR control logic. . This SAR ADC achieves a very low power consumption of 25.58nW and it exhibits good performance and achieves an FOM of 25.68fJ/conversion-step with ENOB of 9.96 bit.

Key References

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