High Performance DDR4 Memory Controller with Adaptive Page Management Policy

Krutika Gulvady, Mahesh Gudivada

Department of Electrical Engineering, San Jose State University, San Jose, California 95192

Introduction

Design and implementation of a low latency memory controller in hardware is a critical requirement for the System On Chip memories to utilize the advancements offered by DDR4 memory module.

DDR4 Advanced Specifications [1]

- works at a low voltage of 1.2V thus saving power,
- faster data speeds of 2133MT/s to 2400MT/s,
- internal bank groups ,
- 8n pre-fetch architecture,
- data bus with CRC check.

Memory Controller Basic features

- Command Generator
- Address mapping
- Data FIFO
- Request Buffers
- Response Buffers

Design Critical Parameters

Timing Parameters

Meeting multiple timing requirements makes design of DDR4 memory controller complex. These include the following among others

- tRAS
- tCL
- tRC
- tRRD
- tREFI

Setting Mode Registers

The memory runs in normal mode by setting default DDR4 parameters by writing in mode registers through the controller. The field written into include

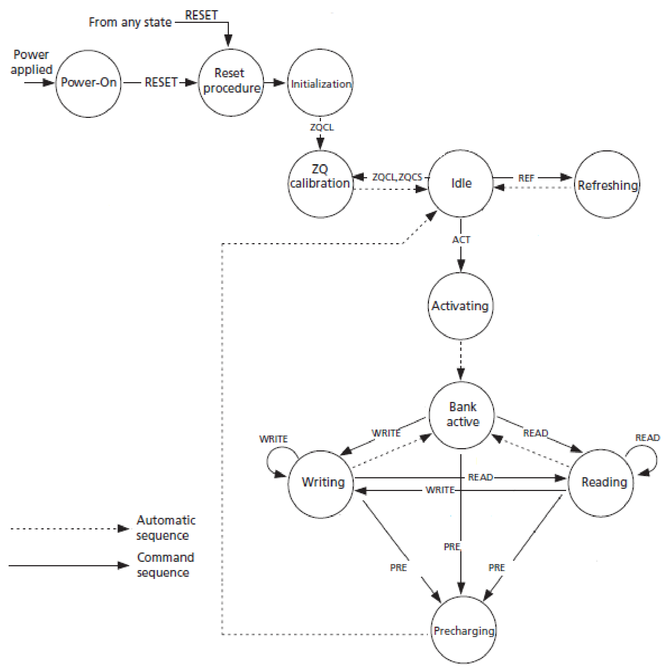
- Burst Type
- Burst length
- CAS Latency
- Write Command Latency
- CRC state

Design Approach

Key Points

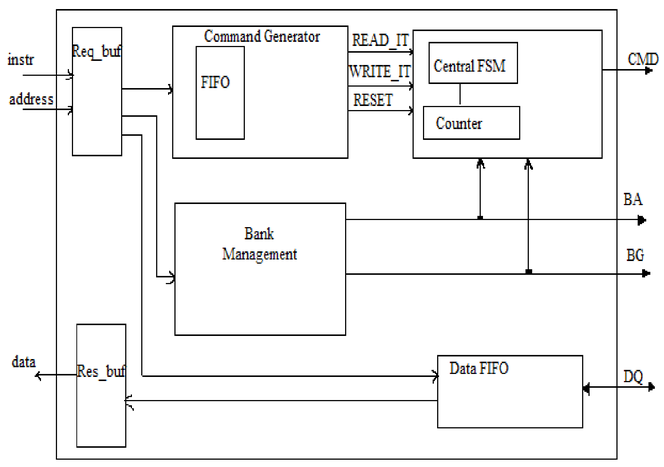
- State Diagram for core controller
- Blocks
- System Verilog

State Diagram for Core Controller



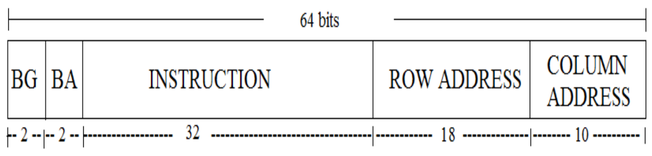
Modified state diagram of core memory controller inspired from Micron DDR4 module[1].

Design Methodology



Block level diagram of design implemented [2].

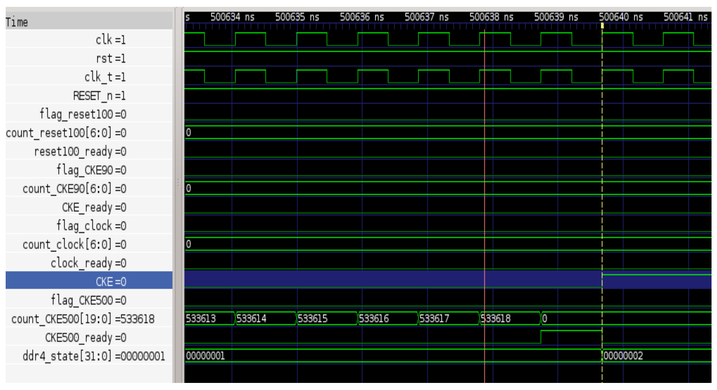
The design works with the instruction and address coming in from the testbench representing the CPU memory access request.



Memory request from the testbench.

Results & Future Scope

Instruction addresses extracted using PERL scripting language code. Used these 64 bit data to introduce address and commands into I/O pins. The command signals are found to be received at the pin interface for memory at the correct timing as per the data sheet of the DDR4 Micron module.

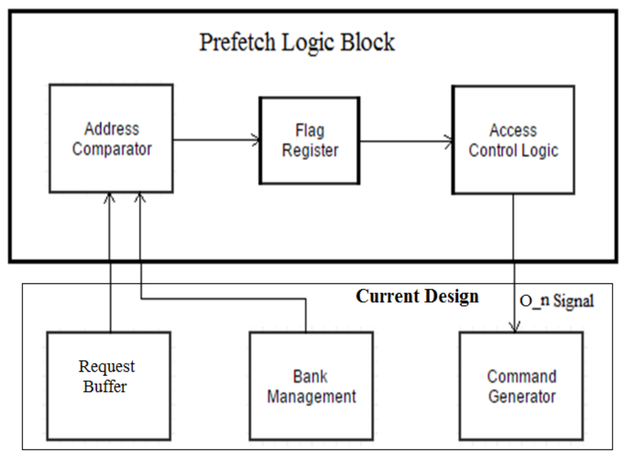


Measurement

The result calculated by dropping markers at the expected time and actual time of arrival of the signals. The CKE goes high at 500.640us which is close to expected value of 500us after adding.

Future Scope – Adaptive Page Management

Reduction in row access latency by predicting the Page Open or Page Close policy in advance [3]. Done using Prefetch Logic block to be introduced in current design.



Conclusions

The project has designed a timing efficient DDR4 memory controller. The basic design of a DDR4 memory has been studied in depth. Design uses synthesizable System Verilog as the language for design, making it unique in terms of design as well as verification. The design can be further modified by targeting the page policy. This project thus largely improves the memory access times for SoCs. This reduced access times increases the performance of the entire system on chip.

Key References

[1] Micron Technology, Inc., "DDR4 SDRAM," 25 October 2014. [Online]. Available: https://www.micron.com/~/media/documents/products/data-sheet/DRAM/ddr4/4gb_ddr4_sdram.pdf.

[2] M. Ringhofer, "Design and Implementation of a Memory Controller for Real-Time Applications," Graz University of Technology, Graz, 2006.

[3] K. Li, Q. Guang, L. Lei, Y.-J. Peng and J.-Y. Shi, "A high-performance DRAM controller based on multi-core system through instruction prefetching," Ningbo, 2011.

Acknowledgments

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For further information

Please contact *krutika.gulvady@sjsu.edu*. System Verilog code, simulation files, memory module files and PERL code are available upon request.