TDC AND DCO noise with no dither added at TDC input

Modeling of TDC based All Digital Phase Locked Loop

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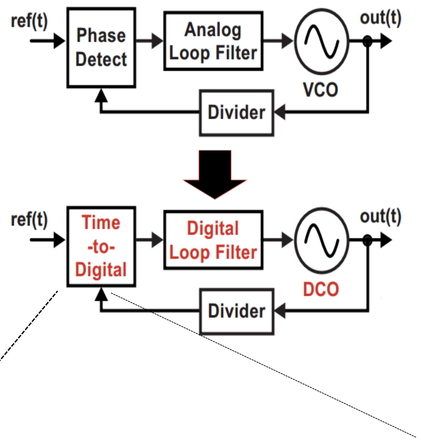
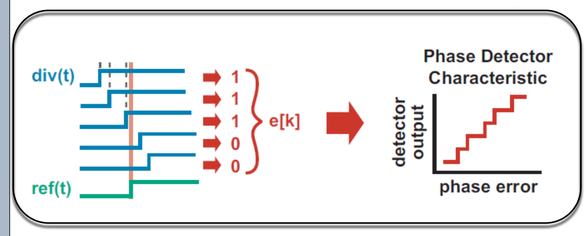
Introduction

An All-Digital Phase Locked Loop (ADPLL) is an alternative approach to a traditional analog Phase Locked Loop (PLL) for implementation in modern Nano-scale CMOS processes. One key advantage of ADPLL is they use digital circuits to achieve the requires filtering in the loop, as compared to bulky analog loop filters that require large capacitors on chip, thus saving a lot of area. Moreover the phase error and other control parameters in the loop are now digital words, produced by digital circuits. This allows for a more attractive digital flow which can be made re-configurable with external assistance through software. Time domain modeling predicts the entire working prior to the actual implementation In this project we model a TDC base ALL digital PLL using MATLAB and Simulink. Using predefined blocks in Simulink environment to model a system reduces the effort of integration in different simulation environments This project focuses on a behavioral model of a TDC based digital PLL. Simulink models are created to efficiently model each block mathematically, to achieve time domain behavior. The design elements include TDC as phase error detector, Digital loop filter and a DCO. The ADPLL is characterized in terms of output frequency, resolution, bandwidth, locking speed and jitter.

Methodology

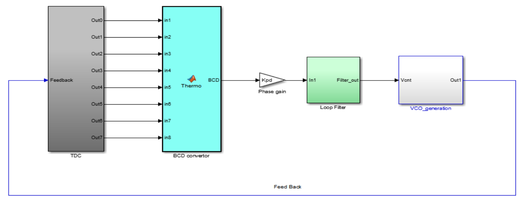
Digital circuits, even though are more complex in nature, are compact, less sensitive to leakage current and PVT variations. Thus digital approach of designing PLLs offer excellent performance with a lower cost of implementation. In recent literature there has been a lot of development and research to push the performance of All Digital PLLs.



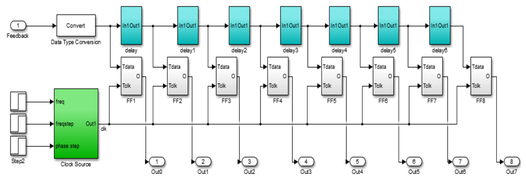


Methodology

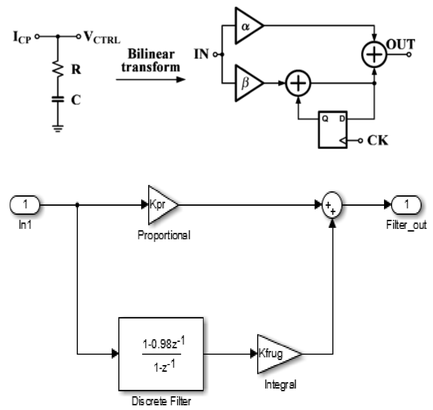
The proposed architecture for modeling of DPLL is shown below. It is similar to conventional PLL with internal blocks replaced by digital circuits.



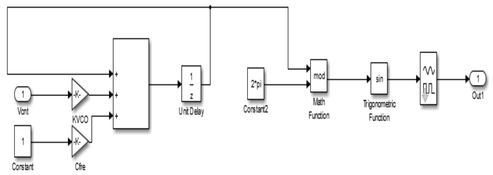
•TDC used as a phase detector in an All-digital PLL. The TDC effectively gives the time difference representation in thermometer code.



The digital filter is implemented using both “proportional” and “integral” path as proposed in [2]. A analog representation of the loop filter converted to digital domain using bilinear transform. Sample period for the digital filter is the reference frequency.

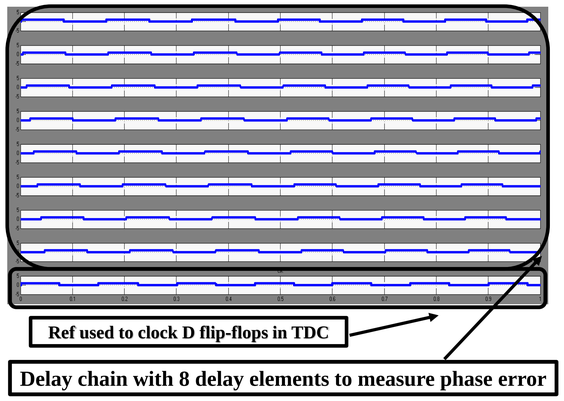


The VCO is modeled by accumulator based approach. The phase at each time step is generated with addition with constant center frequency, the varying phase due to control voltage.

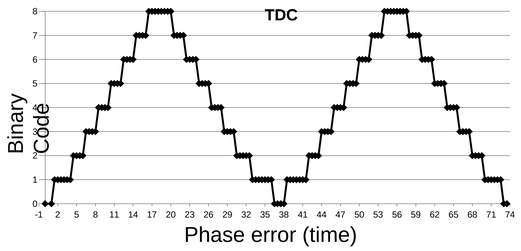


Results

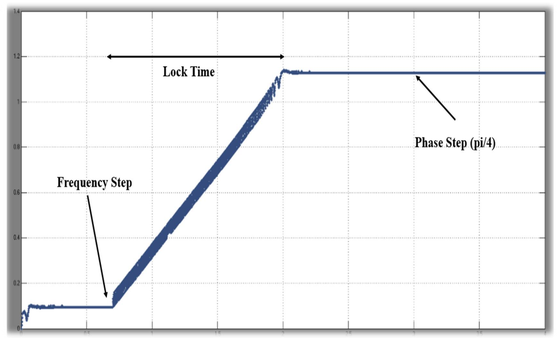
TDC output: The data is delayed by each delay cell with an amount of 1 picoseconds and each flip flop receives the delayed version of prior block.



TDC transfer curve is modeled to act as linear phase detector with quantization error. A plot of time (phase error) v/s binary code generated by the TDC is shown. Thermometer code of TDC is encoded into binary code.

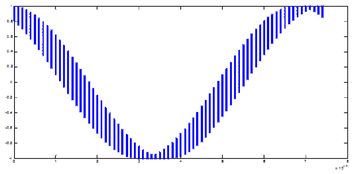


A plot of the control voltage for the simulation period reveals how much time the PLL takes to lock. The PLL was simulated for a frequency step and a phase step.

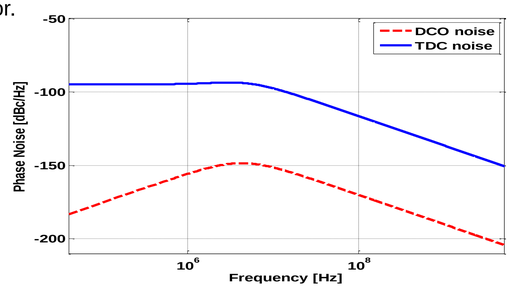


Eye diagram for the simulated PLL

The reported jitter (p-p) is **0.093UI**



A plot of phase noise due to TDC and DCO input is shown. It is seen that the TDC contributes more to the phase noise of the PLL. Thus the design of the TDC is more critical to meet the standard the PLL is designed for.



Summary

Circuits as being Digital, completely analog in nature or a mix of both analog and digital blocks; called mixed signal systems. The kind of system definition defines how the simulator mathematically calculates the results of a system. Thus in a mixed signal system as in the ADPLL, where there is a continuous time to discrete time conversion happening at phase detector and again a discrete time to continuous time conversion happening at VCO.

Key References

[1] B. Razavi, "The Role of PLLs in Future Wireline Transmitters," *Transactions on Circuits and Systems I,* pp. 1786- 1793 , 2009.

[2] M. Perrott, " Tutorial on Digital Phase-Locked Loops," CICC , 2009.

[3] S. Henzler, Time-to-Digital Converters, Springer Series in Advanced Microelectronics, 2010.

[[4] J. Yu, F. FDai and R. C. Jaeger, "A 12-Bit Vernier Ring Time-to-. Digital Converter in 0.13 µ m," *IEEE Journal of Solid-State Circuits,* 2010.

[5] V. Kratyuk, P. K. Hanumolu, U. Moon and K. Mayaram, "Design Procedure for All-Digital Phase-Locked Loops Based on a Charge-Pump Phase-Locked-Loop Analogy," *IEEE Transactions of circuits and systems,* pp. 247-251, 2007.

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