May 2rd, 2014 Thesis/Project Presentation Room 345

Name of each group member	Title	Project Advisor	Project Co-Advisor	TRACK	SECTION	TIME
Rajabhandharaks, D	Control of Hydrostatic Transmission Wind Turbine	Hsu	Mir	1	1	9:00
Gaddam, Chidvila Reddy	Implementation of Black Scholes Optional Pricing model for American Option Style	Choo	Choo	1	1	9:25
Xu,S Ting,A	A Multi-Softcore System for Efficient JPEG Encoder Using FPGA	Choo	N/A	1	1	9:50
Mansi Chhichhia Prachi Gangote	Nand Based Flash Memory Controller with NOR Improvements	Jones	N/A	1	1	10:15
Samskruthi Devendran	Architectural study on the effectivness of a single line buffer	Jones	Caohuu	1	2	10:50
Jaafari, S.	Adaptive Filtering for Heart Rate Signals	Ardalan	Zaragoza	1	2	11:15
Agale P	Low voltage Continuous time linear equalizer	Ardalan	Jones	1	2	11:40
Gustavo T. Villanueva	10 GHz Adaptive Receiver Equalization Design	Ardalan	Hamedi-Hagh	1	2	12:05
lunch	**lunch**	**lunch**		**lunch**	**lunch**	**lunch**
Ali, M	Low Power A-D Converter Design for Software-Defined Radios	Ardalan	Hamedi-Hagh	1	3	13:00
Alfred Sargezisardrud	Delay F/F (DFF) Metastability Impact on Clock and Data Recovery (CDR) and Phase-Locked Loop (PLL) Circuits	Ardalan	Hamedi-Hagh	1	3	13:45
Danyom Berhane	Design of a Printed Antenna for LTE	Hamedi-Hagh	Shahab Ardalan	1	3	14:30
Mane R	Design of Mixer And LNA for RF Receiver Circuits	Hamedi-Hagh	N/A	1	3	14:55
Kabir, F.	Design of a Ku Band LNB using 45nm technology	Hamedi-Hagh	N/A	1	4	15:30
Nguyen Dung	Design a High Performance Arbiter for ML-AHB Bus	Le	Le	1	4	15:55

May 9th, 2014 Project Presentation

Name of each group member	Title	Project Advisor	Project Co-Advisor	Track	Section	Time
	TRACK 1 Room EE345					
Anirudh Sri Jayendra	Packet Filtering Technique on Router Based on Protocol Type	Mir	Mir	1	1	9:00
Panjari, Yash Chandnani, Alenka	Simulation of a Campus Network Using SDN	Mir	Mir	1	1	9:25
Aboli Pimpalkhare Aniruddha Vyawahare	Packet Filtering at Routers	Mir	Mir	1	1	9:50
Suresh Kumar, Pradeep balaji Tharuvai Srinivasan, Anand Kumar	Netgear Privacy and Advertising Platform	Mir	Mir	1	1	10:15
Sunkara, P. Manikonda, H.	Implementing SDN in Data center environment using OpenDaylight and OpenFlow standards	Mir	Mir	1	2	10:50
Bui, Dennis ; Danala, Punitha	Experimenting with Load Balancing for a Cloud Computing Network	Mir	Lin	1	2	11:15
Fazel, A. Mehdi-Ghiastalab, N.	A Simulation of Information Centric Networking (ICN)	Mir	Lin	1	2	11:40
Badisu, C. Gudavi Vijaykumar, C.	Simulation of Traffic Load Balancing in High-speed Cloud Network	Mir	Lin	1	2	12:05
lunch		**lunch**	**lunch**	**lunch**	**lunch**	**lunch**
Priyanka Kumar Silpa Cherravuru	Analysis of Improvement in Multimedia service Using Load Balancing	Mir	Mir	1	3	13:00
Santhosh Kumar Pattabhiraman Bhavin Mehta	Netgear Privacy and Advertising Platform	Richard Sinn	Mir	1	3	13:25
Aloorkar,P. Jagtap, A.	SDN based Network Monitoring Application	Chao-Li Tarng	Mir	1	3	13:50
Amogh Gawade Nikita Naik	Application Aware Routing	Chao Li Tarng	Jones	1	3	14:15
HM, S. Bendale, U.	Openstack Topology Orchestration	Chao-Li Tarng	Jones	1	4	14:50
Bumb. P.	BIST for NAND Flash Memory	Jones	N/A	1	4	15:15
Shah, P. Sawantdesai, J.	Automated adaptive multicore machine based on cache hit-miss rate for power efficiency	Jones	N/A	1	4	15:40
Kane, S. Pandit, C.	Functional Verification of MIPS core using UVM	Jones	N/A	1	4	16:05
	TRACK 2 Room EE341					
Gajipara,Pooja Girigowda,Pavan	Non Volatile Memory (SSD Controller) Interface Design	Choo	Jones	2	1	9:00
Gondalia,R.	Recursive Least Squares Algorithm for Noise Cancellation on FPGA	Choo	Choo	2	1	9:25
Gupta, Akshat Takodara, Vishal	Smart Sensing	Choo	Jones	2	1	9:50
konda varun kumar reddy	NAND FLASH controller	Choo	Jones	2	1	10:15
Patwardhan S Pimplapure R	Functionality and Performance Verification of Memory Controller	Jones	Jones	2	2	10:50

Rajesh Subramanian,F Pareek,S	UVM verification of 8051	Jones	N/A	2	2	11:15
Deshpande, V. Sakhalkar, S.	Adaptive Verification Methodology for targeted Functional Coverage	Jones	N/A	2	2	11:40
Bangalore Lakshman, S. Mangrulkar, V.	A scalable accelerated verification methodology for verification of Embedded SoC IP	Jones	N/A	2	2	12:05
lunch		**lunch**	**lunch**	**lunch**	**lunch**	**lunch**
Kuo, C. Zhang, Y.	Hardware Design of Color Balancing and De-Blurring Algorithm for Wearable Image Capture Devices	Choo	N/A	2	3	13:00
Ryot, A. Gholba, S.	FPGA prototyping of low power audio codec for wearable devices	Choo	Jones	2	3	13:25
Vanam Rohit Kumar Ramanathan Raghuraman	FPGA-Based Hardware Design of True Random Number Generator for Security Applications	Choo	Jones	2	3	13:50
Abhishek Chowdasandra	FPGA implementation of Low Power LCD/TFT Display	Choo	Jones	2	3	14:15
Agrawal, Anuj Suvarna, Prateik	Multicore System Education Using FPGA Prototype Designs for DSP Applications	Choo	Jones	2	4	14:50
Mehta D.	Advanced Programmable Interrupt Controller	Choo	N/A	2	4	15:15
Khatri, K	A cost effective approach for estimating number of people in images	Choo	Jones	2	4	15:40
Qazi, S.	ASIC Implementation and Performance Analysis of Randomized Alamouti Space-Time Block Code In a Cooperative Distributed System	Sirkeci	Jones	2	4	16:05
	TRACK 3 Room TBA					
Vikrant Sarle	Host Adapter design for the Hybrid Memory Cube	He	Jones	3	1	9:00
Dhulipati, S.	Low Jitter PLL using DAC for SerDes transmitter	He	Jones	3	1	9:25
Bindigan Hariprasanna,Abhiram Prasad Rajeswari, Shreyas	The Study and Implementation of Expensive Operations of Monte-Carlo Photon Transport Problem on FPGA	Le	Jones	3	1	9:50
Chinnikannu, Swetha	Implementation of Mersenne Twister random number generator on FPGA	Le	Jones	3	1	10:15
Navya Teja Goda	Development of an Effective Technique to Implement Gaussian Random Number Generator on FPGA	Le	Jones	3	2	10:50
Kadamandla, S	Implementing an Exponential Variate Generator on FPGA	Le	Jones	3	2	11:15
Ramshankar, V	Implementation of the PageRank Algorithm in FPGA	Le	Jones	3	2	11:40
Doshi, N. Bhardwaj, S.	Digital Phase Locked Loop for High Speed Wire-line Link	Ardalan	Jones	3	2	12:05
lunch		**lunch**	**lunch**	**lunch**	**lunch**	**lunch**
Ng, Christopher	Generic Projects with Analog Peripherals for Embedded Systems	Ardalan	Jones	3	3	13:00
Isaac, J.	A Time-Interleaved SAR ADC	Ardalan	Hamedi-Hagh	3	3	13:25
Su Xing	Micorstrip antenna array in beamforming configuration for SISO system	Ardalan	Hamedi-Hagh	3	3	13:50
Devraj Karthikeyan	A 10GHz Narrowband CMOS 4-Bit Phase Shifter	Hamedi-Hagh	Ardalan	3	3	14:15
Nerlikar S. Shendre A.	Implementation of Digital Error Correction in Pipelined ADC	Hamedi-Hagh	Jones	3	4	14:50
Jason Wu	Frequency Lock Loop for LEDs	Hamedi-Hagh	Jones	3	4	15:15